

Compal Confidential

Schematics Document

Intel Chief River Platform

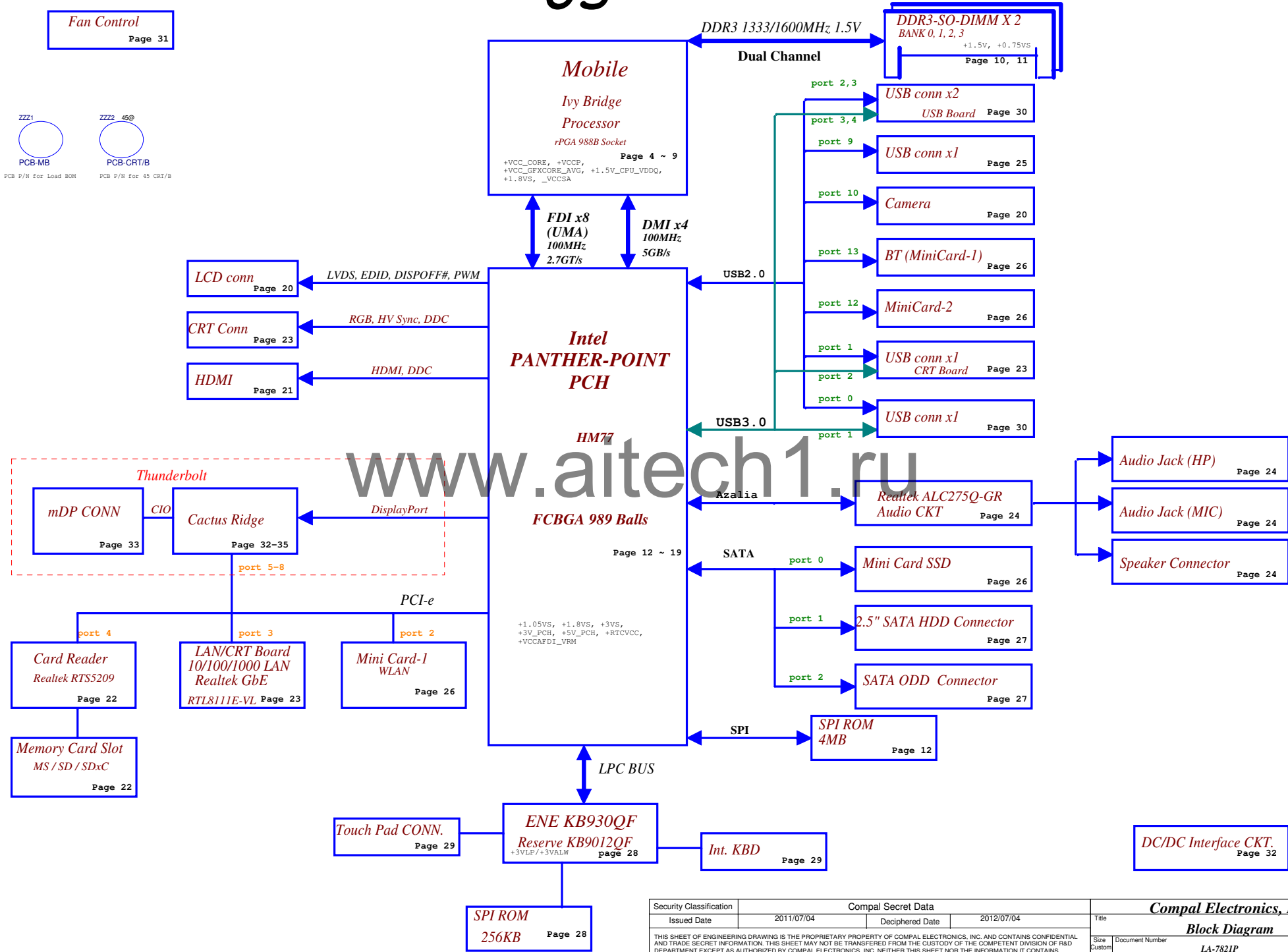
www.sitech1.ru

LA-7821P

2011-07-04

REV: 0.1

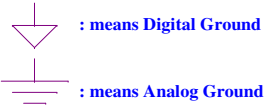
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Issued Date	2011/07/04	Deciphered Date	2012/07/04	Title		
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Voltage Rails (O MEANS ON X MEANS OFF)

<div>power plane</div> <div>State</div>	+RTCVCC	B+	+5VALW +3VALW	+3V_PCH +5V_PCH	+VCCP +1.05VS	+1.5V	+5VS +3VS +1.5VS +VCC_GFXCORE +VCCP +CPU_CORE +1.8VS +0.75VS +VCCSA +1.5V_CPU_VDDQ
S0	O	O	O	O	O	O	O
S3 / DC	O	O	O	O	X	O	X
S3 / AC	O	O	O	O	X	O	X
S3 / S4 / S5 WoLAN	O	O	O	O	X	X	X
S5 S4/AC	O	O	O	O	X	X	X
S5 S4/ Battery only	O	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X	X

Symbol Note :



@ : means just reserve , no build
CONN@ : means ME part.
930@ : means EC KBC930
9012@ : means EC KBC9012

Install below 45 level BOM structure for ver. 0.1

45@ : means just put it in the BOM of 45 level.

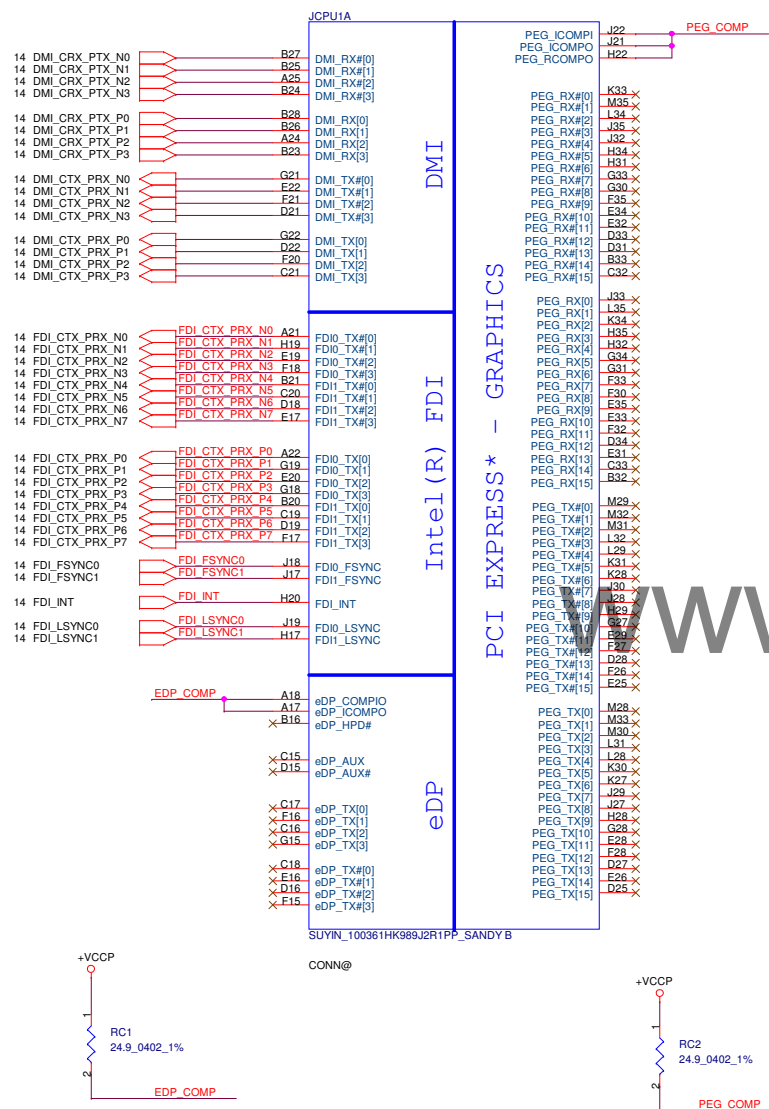
Install below 43 level BOM structure for ver. 0.1

U5 Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	26.1K +/- 5%	0.6191 V	0.683 V	0.7526 V
2	34.8K +/- 5%	0.7745 V	0.8519 V	0.9358 V
3	46.4K +/- 5%	0.9801 V	1.0459 V	1.1133 V
4	56.2K +/- 5%	1.1136 V	1.1873 V	1.2627 V
5	71.5K +/- 5%	1.2918 V	1.3758 V	1.4615 V
6	NC	2.500 V	3.300 V	3.300 V
7				

SMBUS Control Table

	SOURCE	BATT	XDP	SODIMM	EC-KB930	Cactus Ridge	PCH
SMB_EC_CK1 SMB_EC_DA1	EC	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	EC	X	X	X	X	V	V
SMBCLK SMBDATA	PCH	X	V	V	X	X	X
SML0CLK SML0DATA	PCH	X	X	X	X	X	X
SML1CLK SML1DATA	PCH	X	X	X	V	X	X



PCI EXPRESS* - GRAPHICS

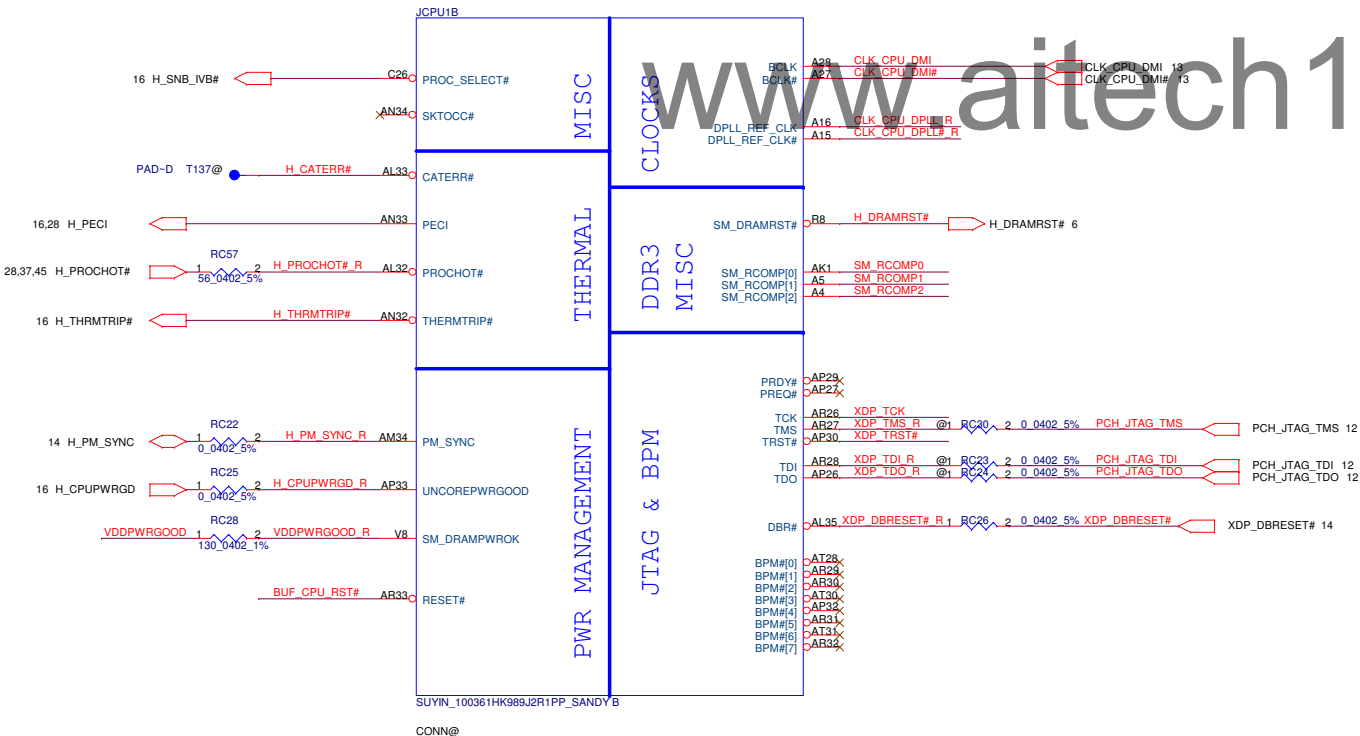
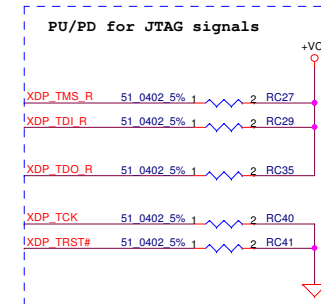
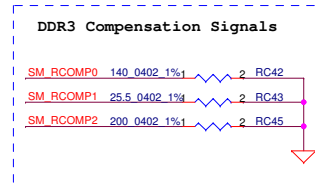
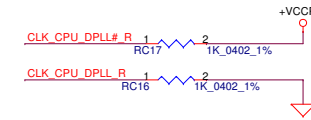
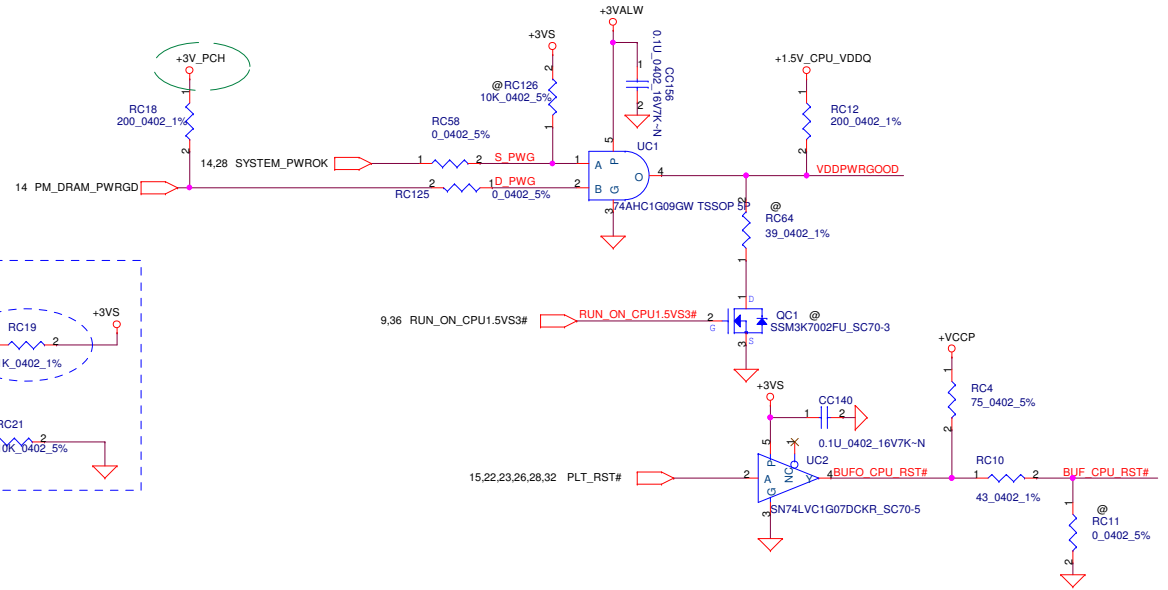
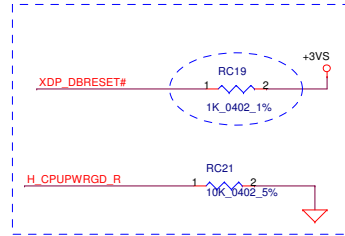
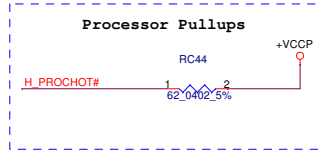
VSS

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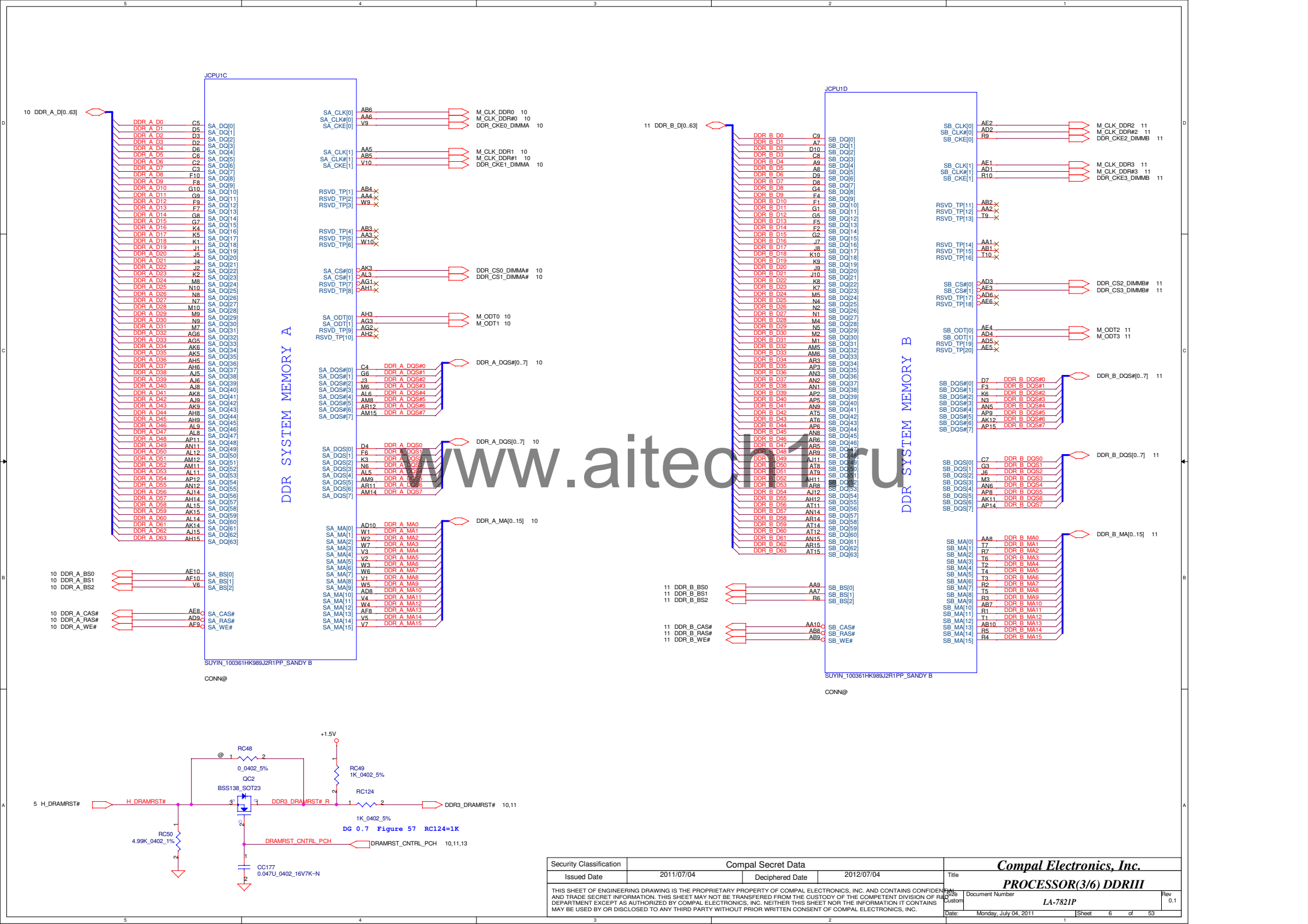
eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms

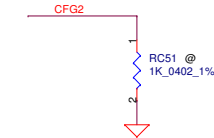
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Issued Date	2011/07/04	Deciphered Date	2012/07/04	PROCESSOR(1/6) DMI,FDI,PEG	
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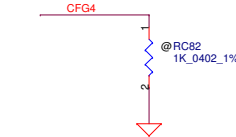
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						Docu- ment Number		LA-7821P		Rev	
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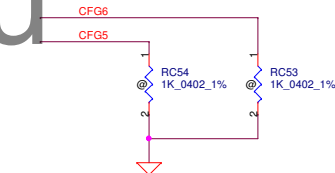
CFG Straps for Processor



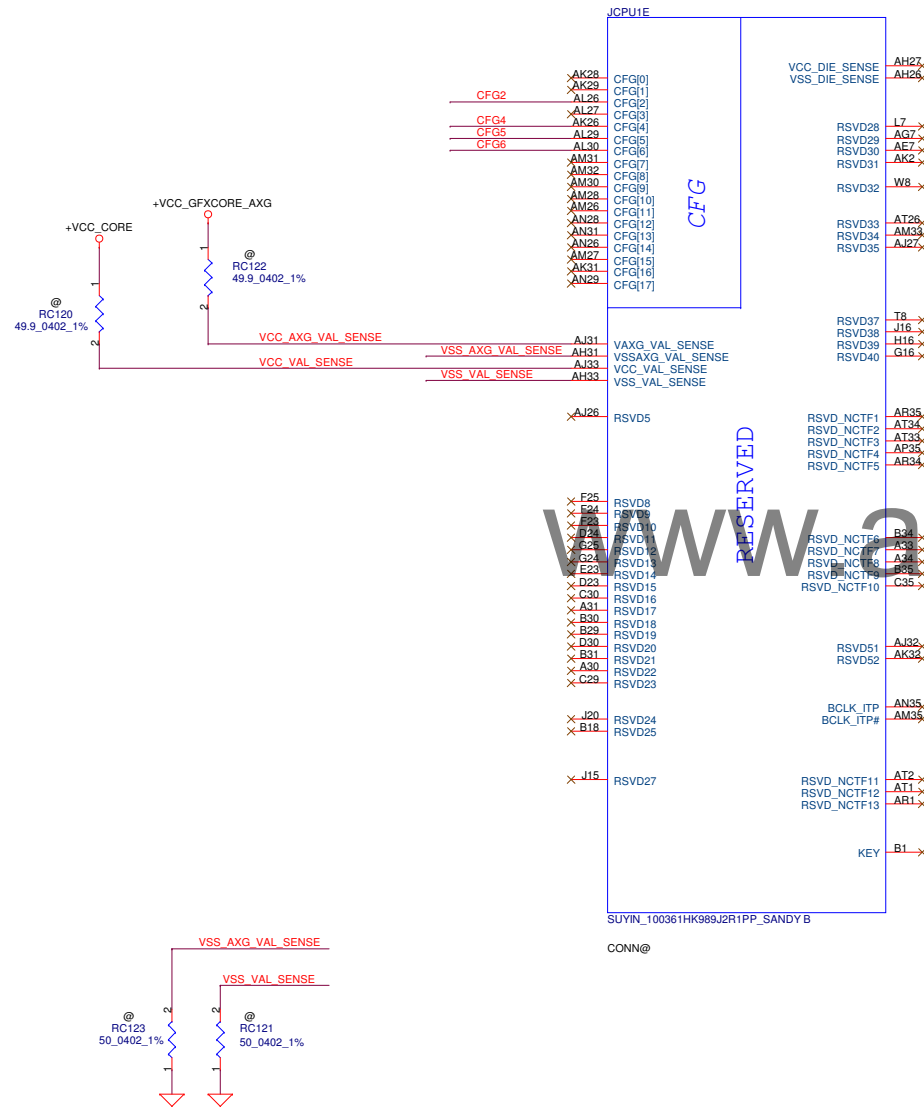
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

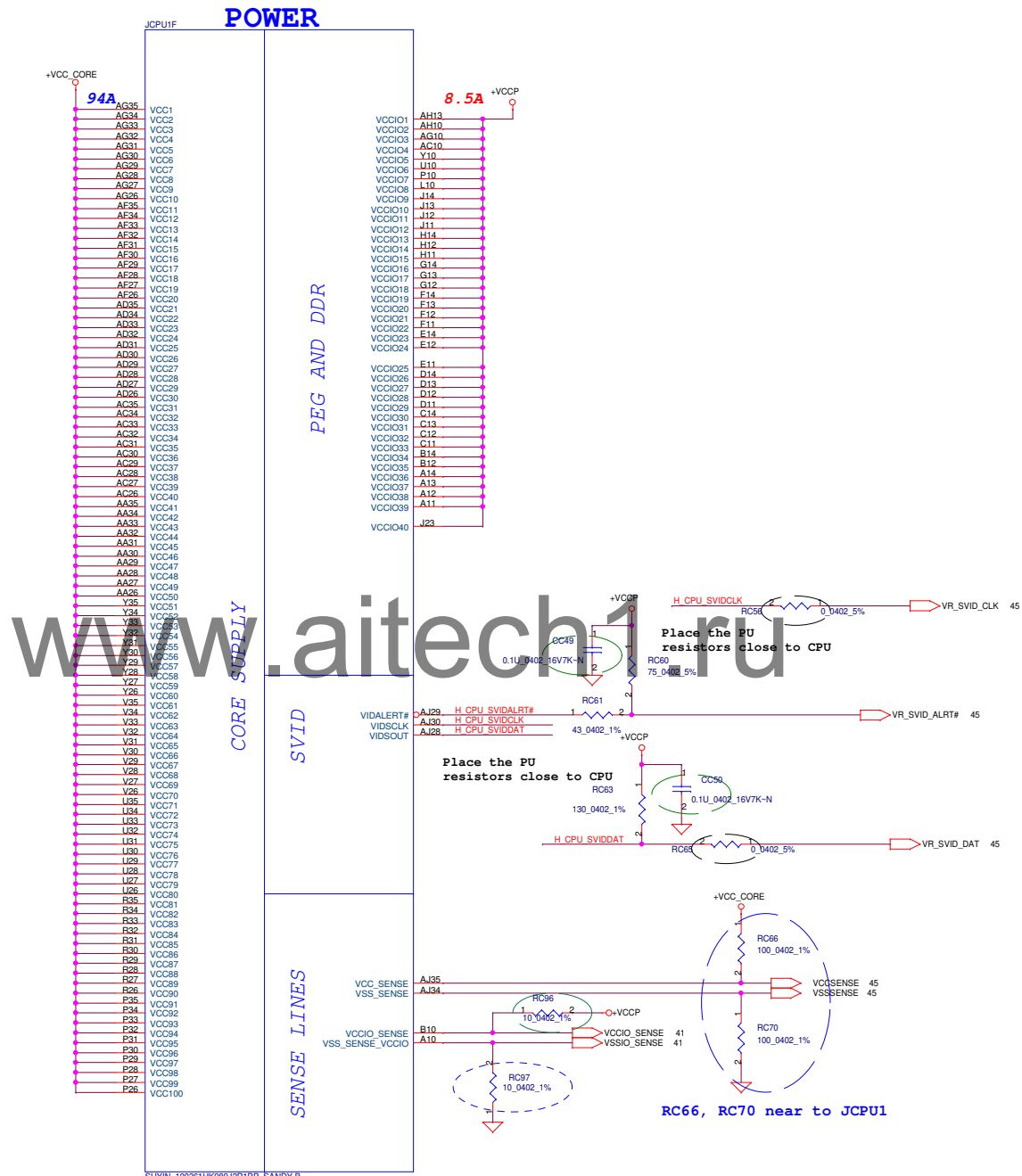


Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



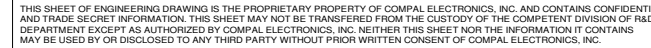
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled





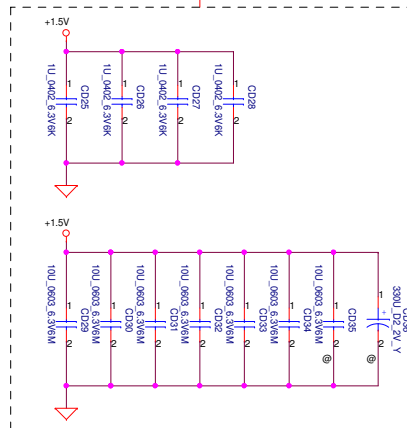
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		Custom		Document Number	
				LA-7821P	
				Rev	
				0.1	
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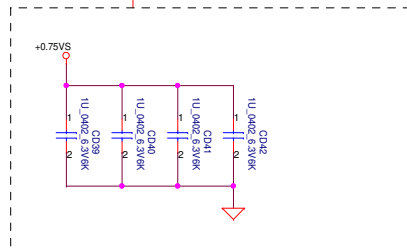


6 DDR_B_DQS#[0..7]
6 DDR_B_DQS#[0..7]
6 DDR_B_DQ[0..63]
6 DDR_B_MA[0..15]

Layout Note:
Place near JDIMM2

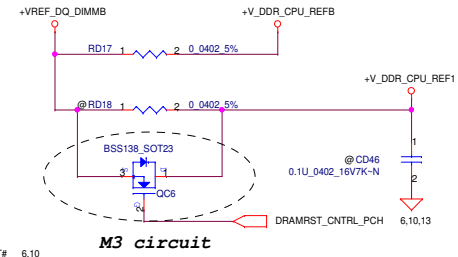
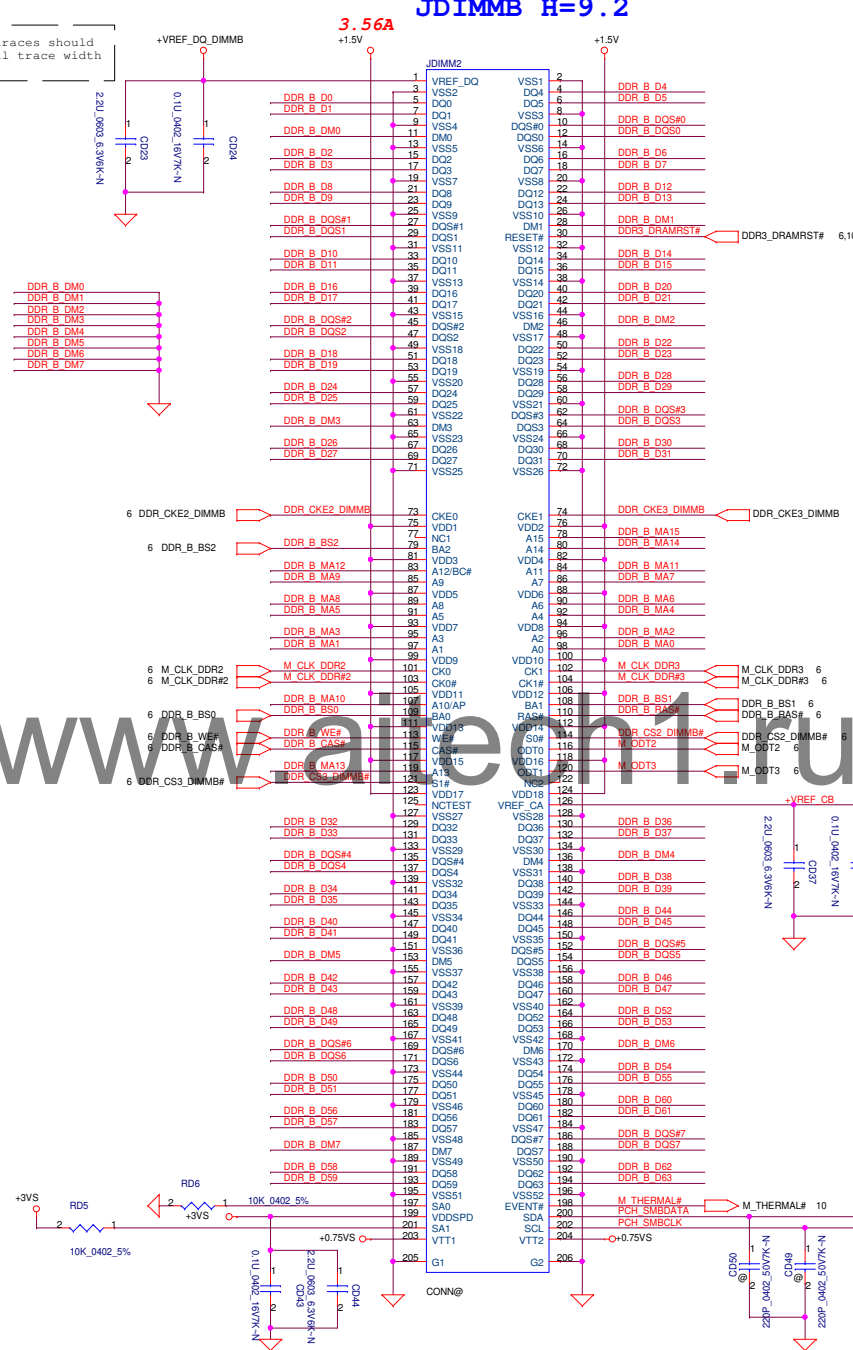


Layout Note:
Place near JDIMM2.203,204



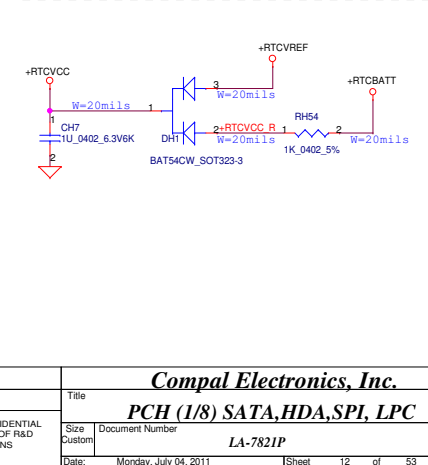
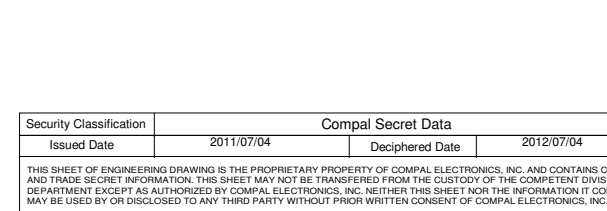
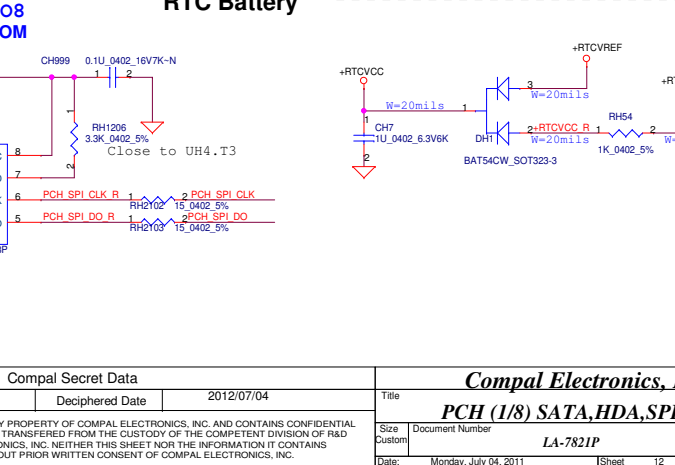
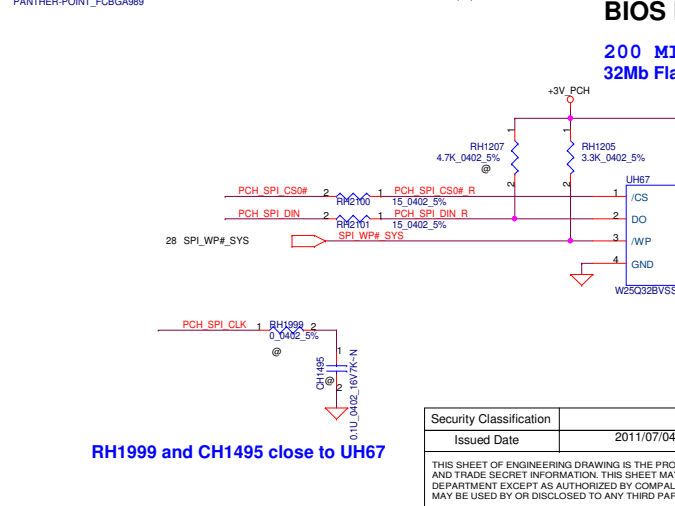
All VREF traces should
have 10 mil trace width

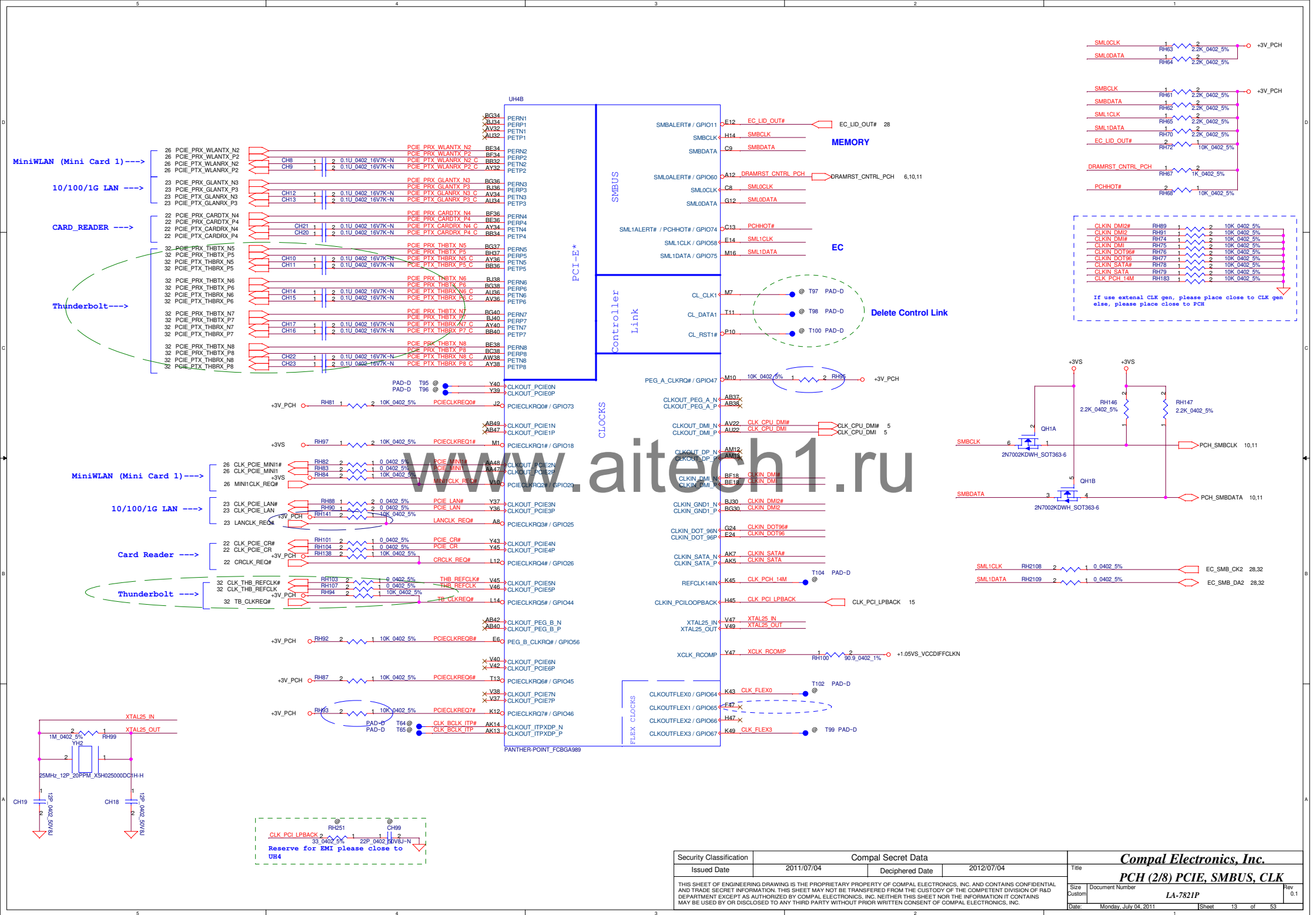
DDR B DM0
DDR B DM1
DDR B DM2
DDR B DM3
DDR B DM4
DDR B DM5
DDR B DM6
DDR B DM7

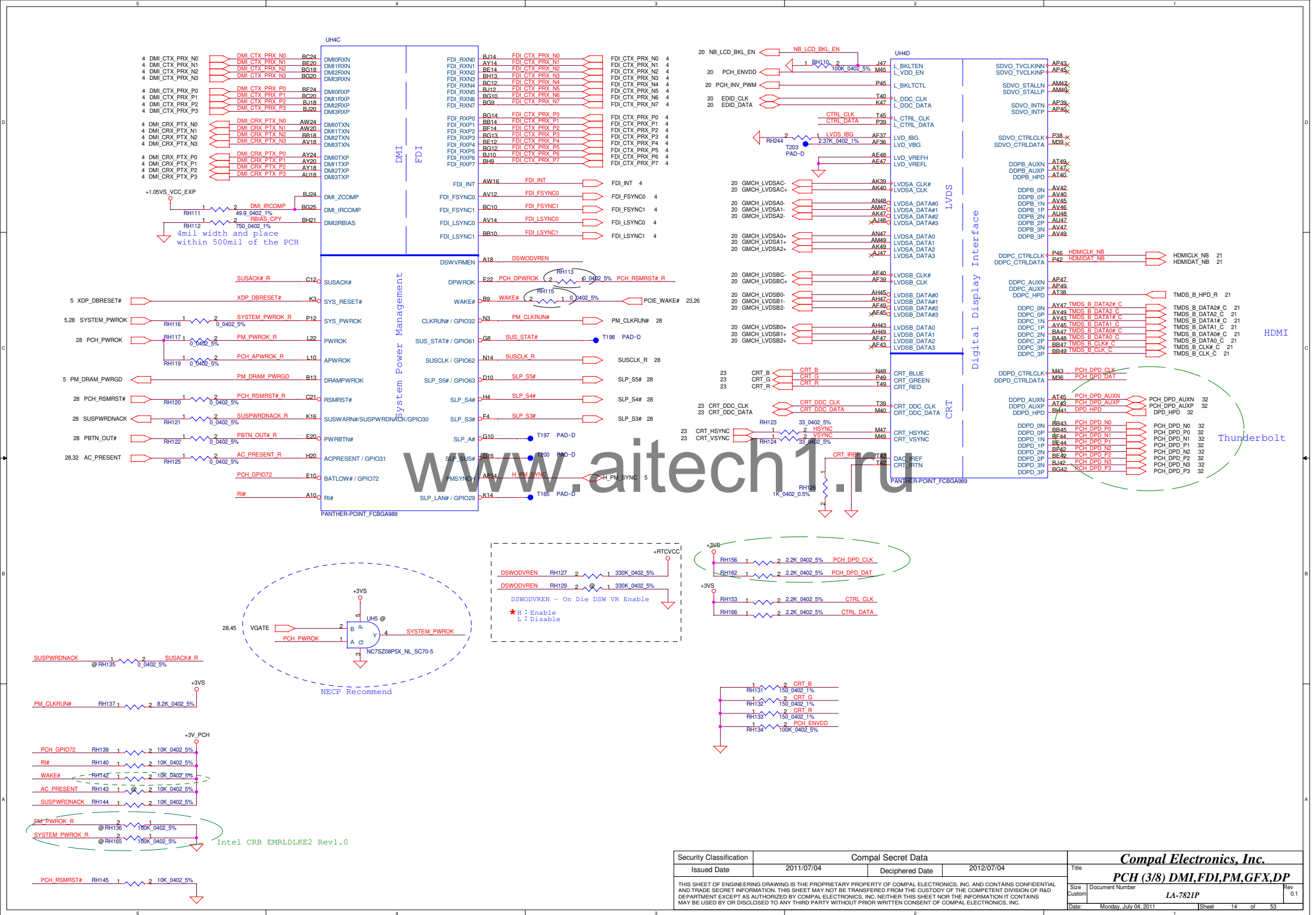


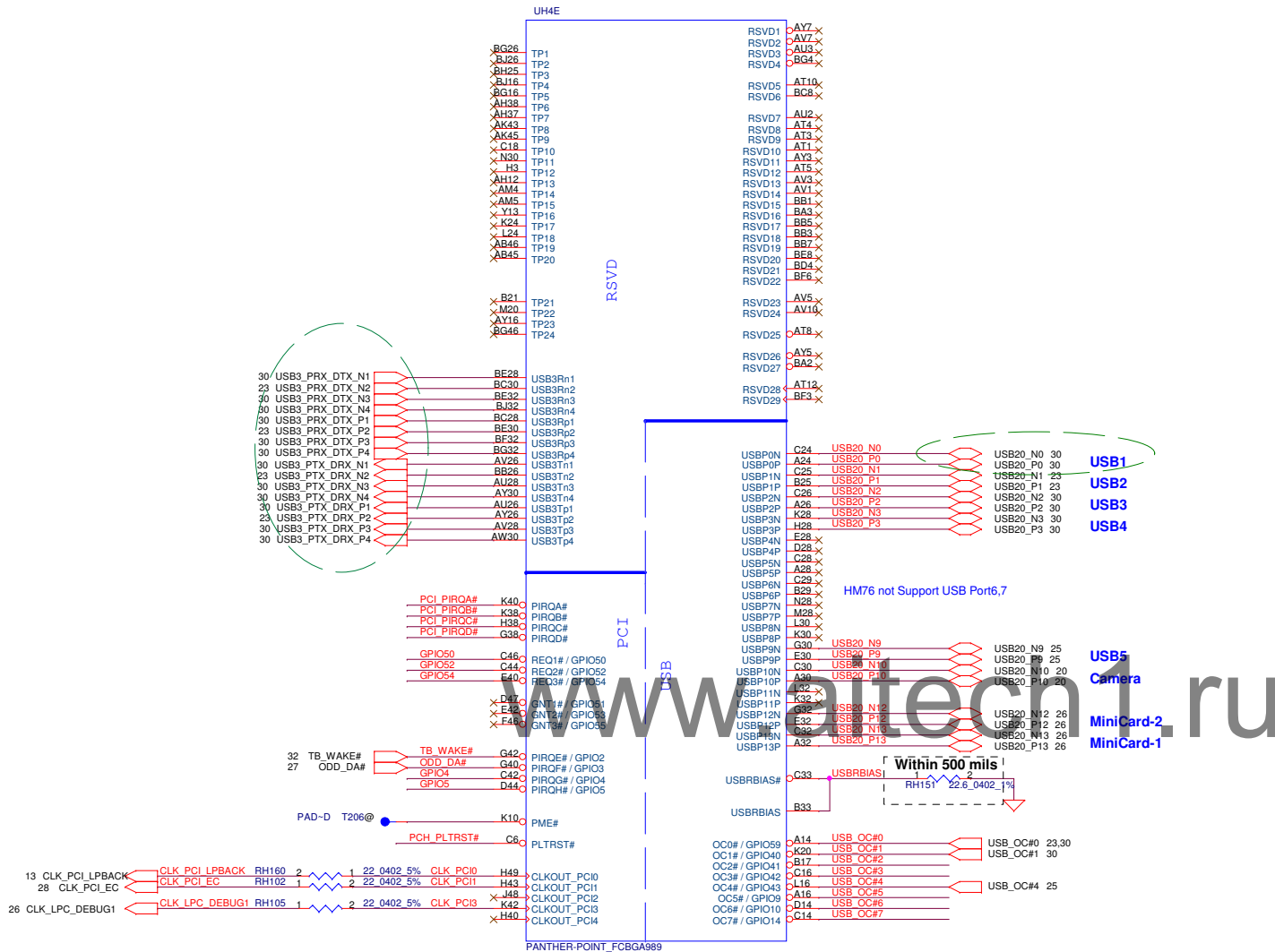
CD49,CD50 close to
PIN200,202

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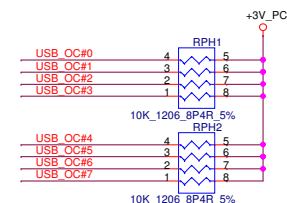
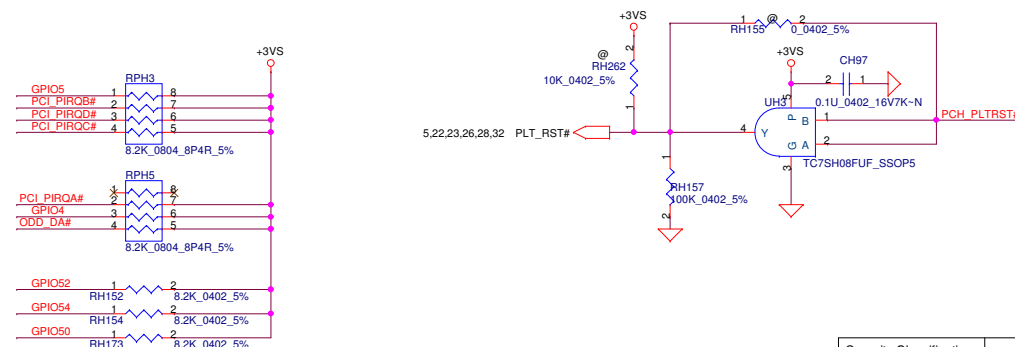


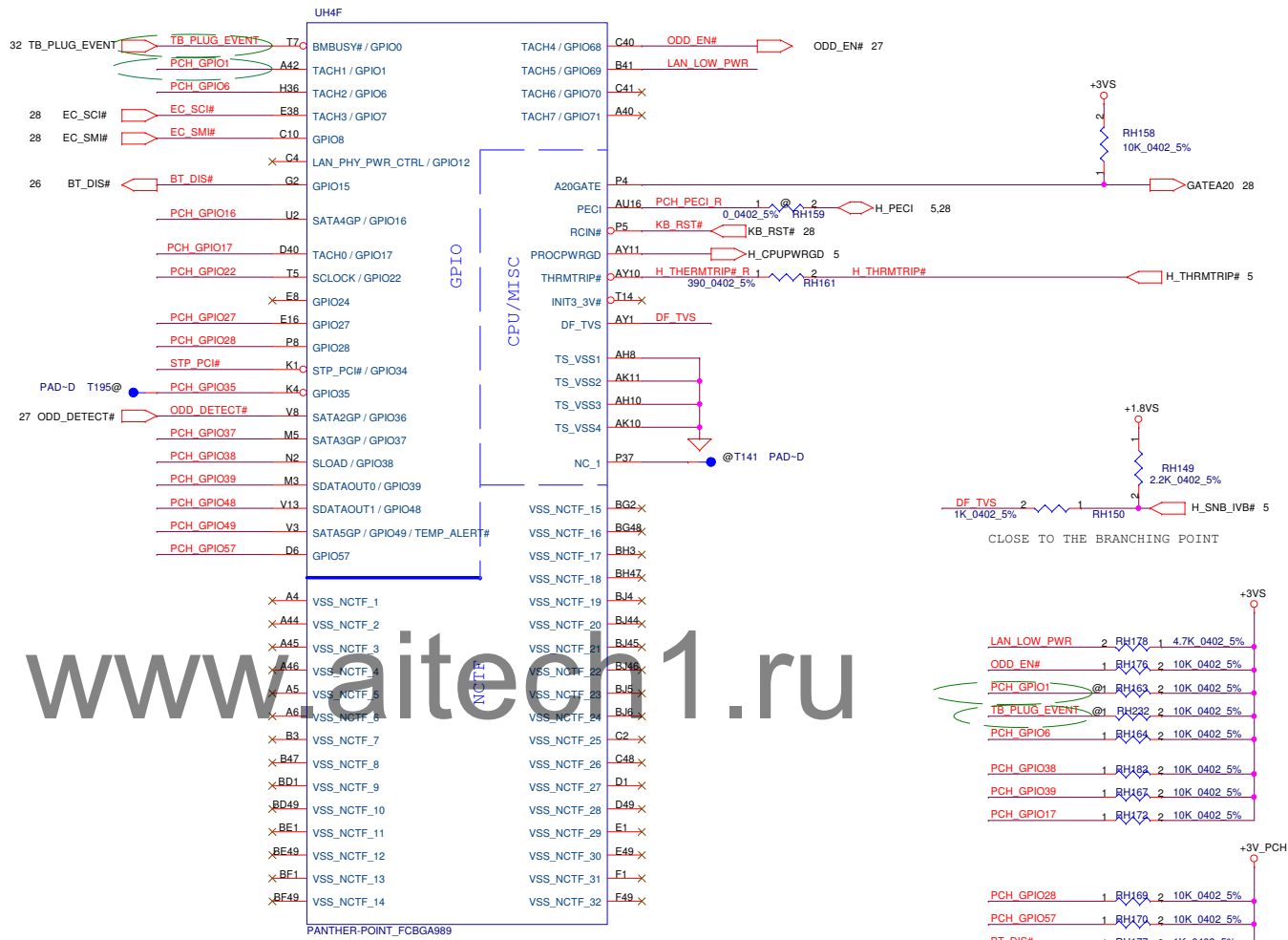
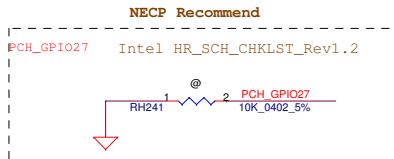
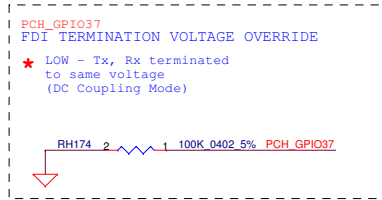
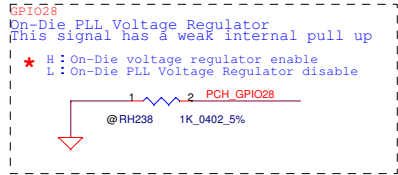
Panther Point USB Port Mapping

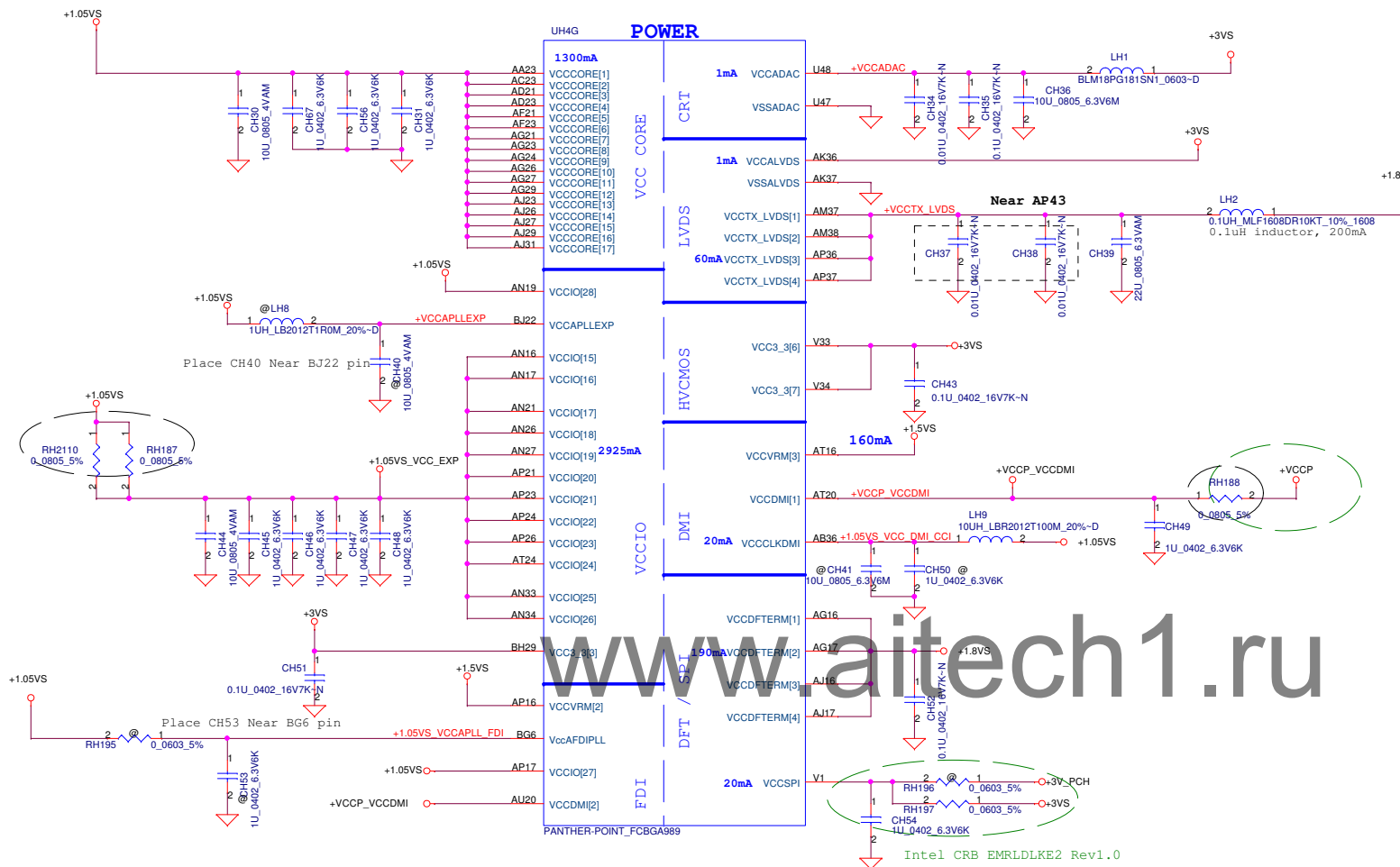
USB 2.0 Port Number	USB 3.0 Port Number
0	1
1	2
2	3
3	4

Over Current Pin Default Usage

OC Pin	PCH Mapping
0	Port 0 & 1
1	Port 2 & 3
2	Port 4 & 5
3	Port 6 & 7
4	Port 8 & 9
5	Port 10 & 11
6	Port 12 & 13







PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.0	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccLVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

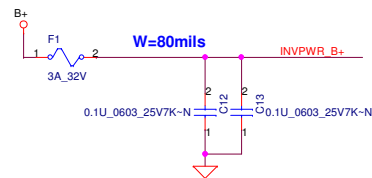
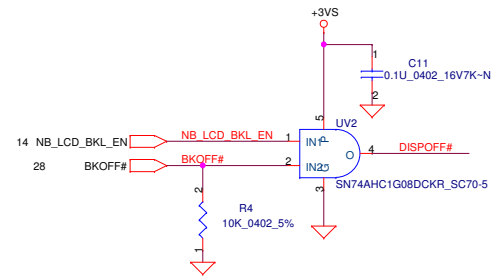
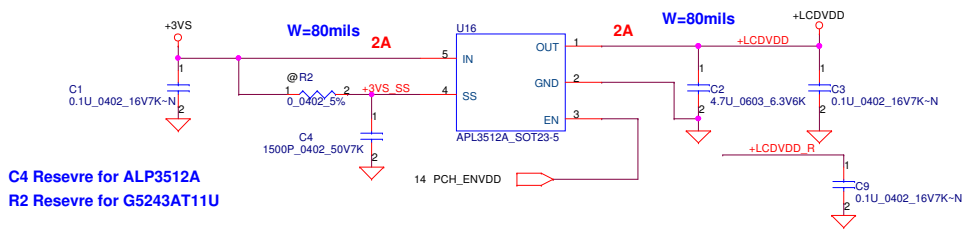


AR48
 VSS[120] AT11
 VSS[121] AT13
 VSS[122] AT18
 VSS[123] AT22
 VSS[124] AT26
 VSS[125] AT32
 VSS[126] AT39
 VSS[127] AT43
 VSS[128] AT47
 VSS[129] AT34

BF28 VSS[206]
 BF33 VSS[207]
 BF30 VSS[208]
 BF38 VSS[209]
 BF40 VSS[210]
 BF47 VSS[211]
 BG17 VSS[212]
 BG21 VSS[213]
 BG33 VSS[214]
 BG44 VSS[215]

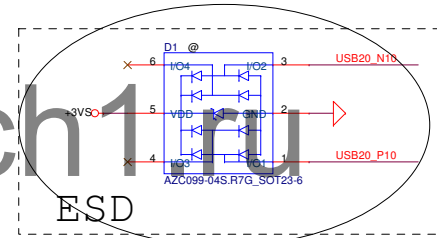
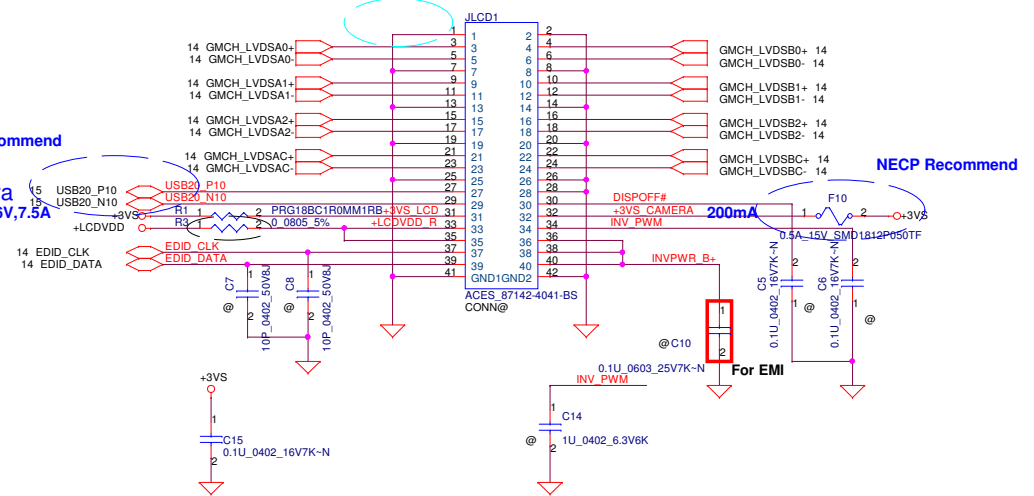
LCD

LCD POWER CIRCUIT

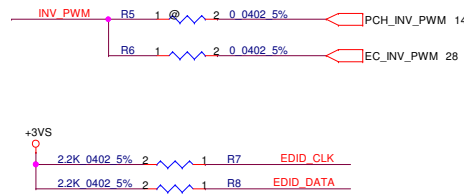
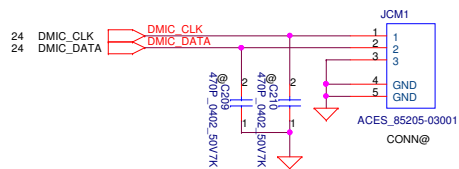


NECP Recommend

Camera
R1: DC=6V,7.5A

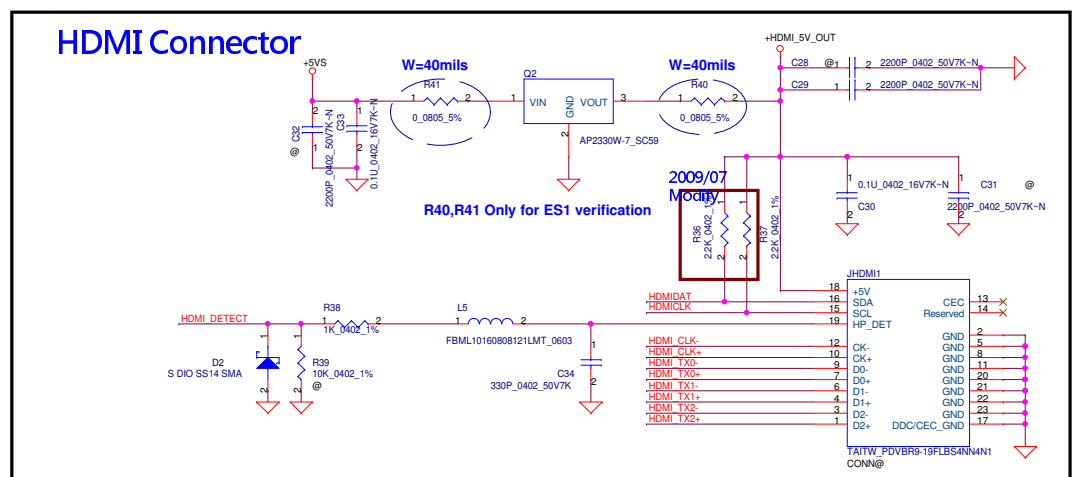
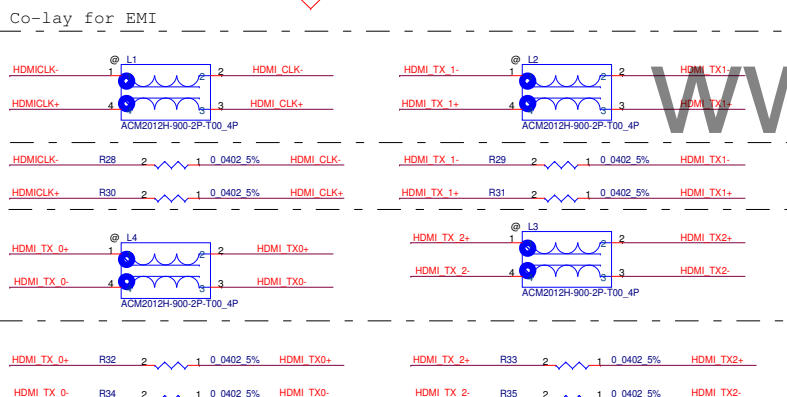
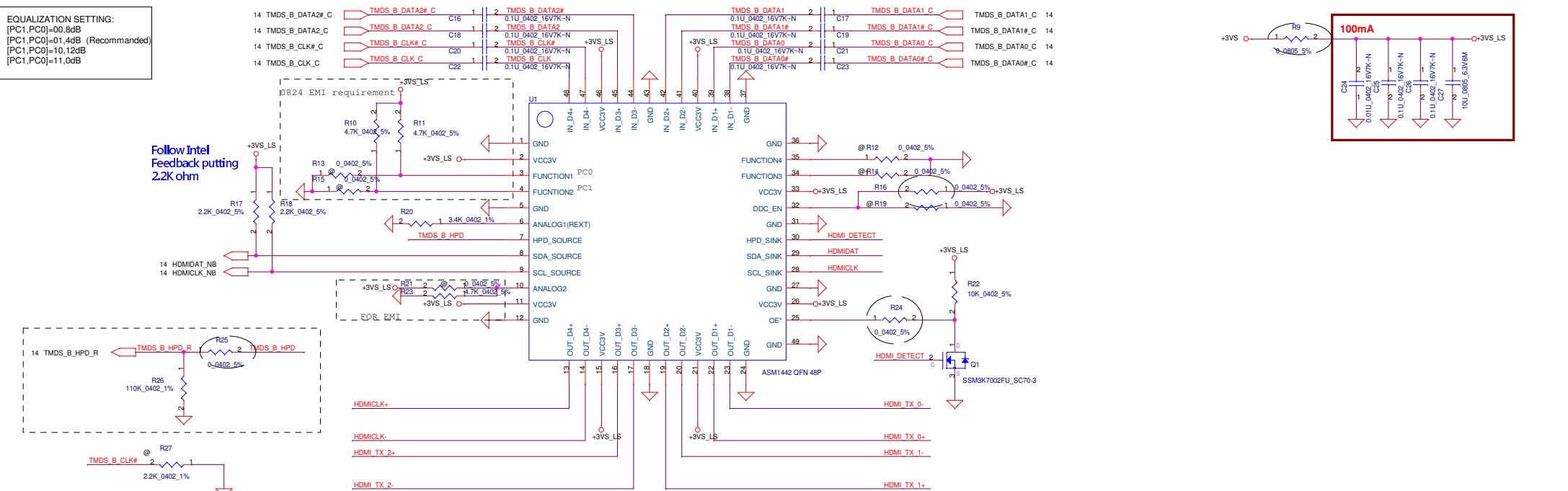


CAMERA

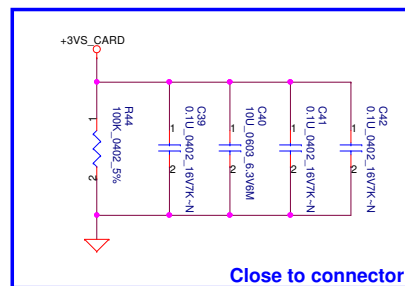
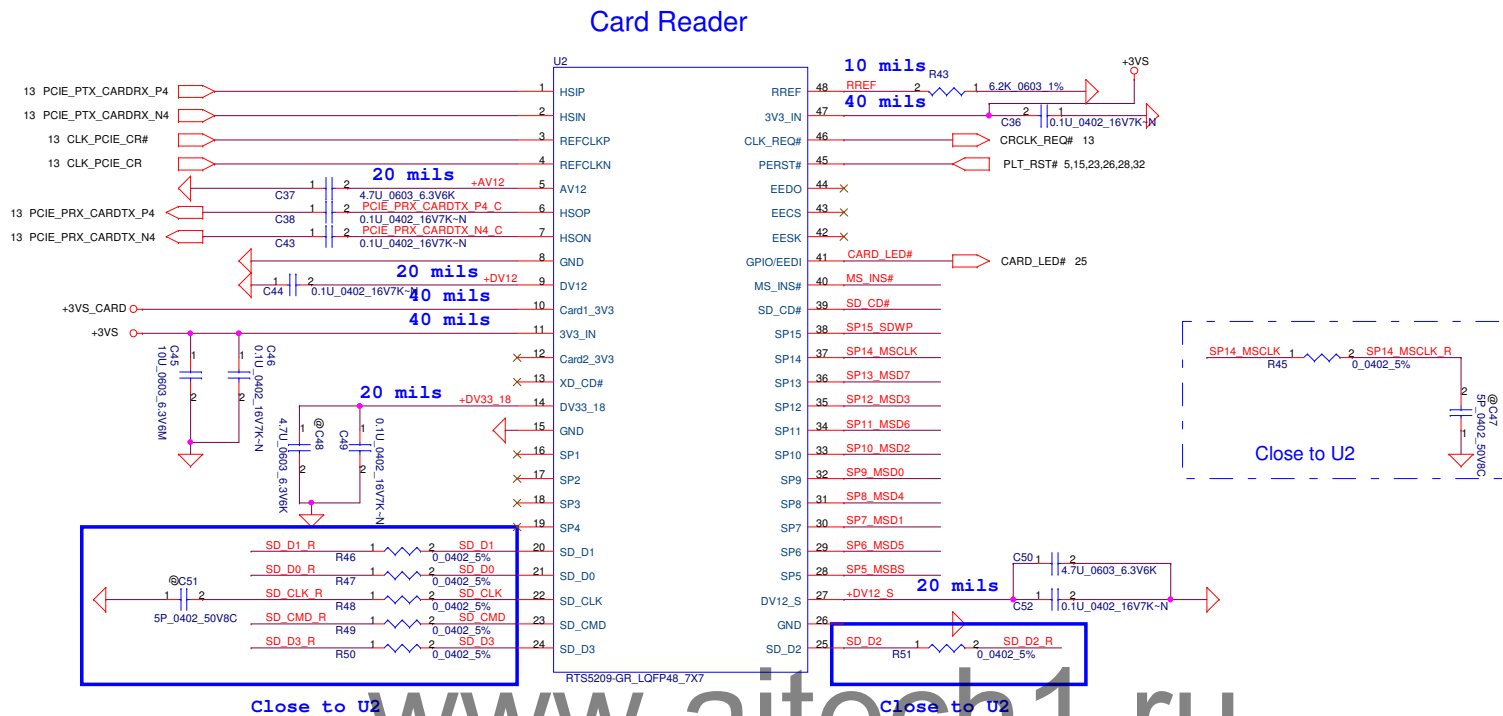


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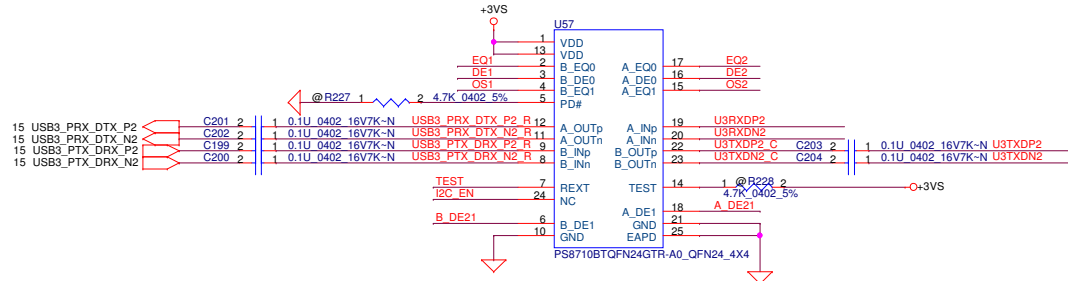
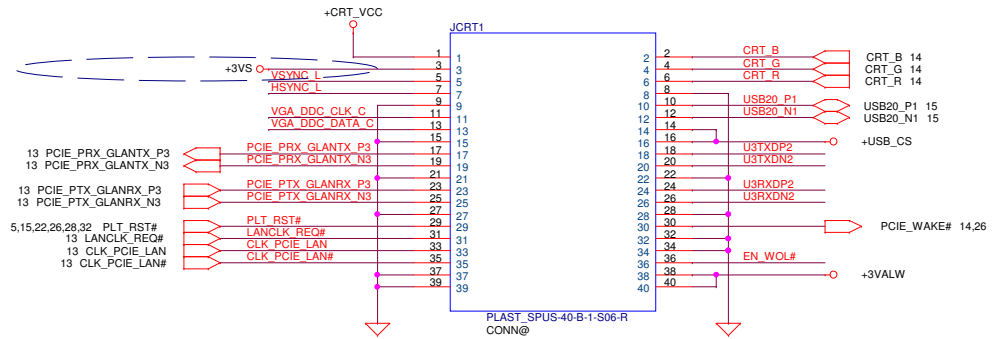
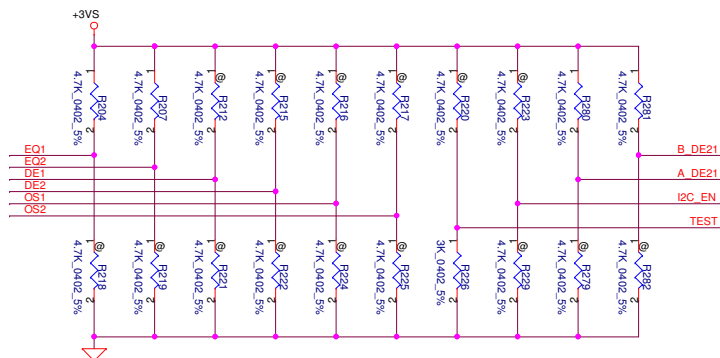
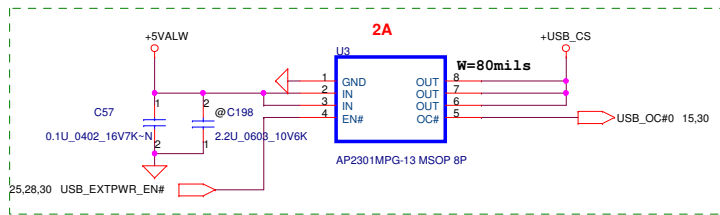
EQUALIZATION SETTING:
[PC1,PC0]=00,8dB
[PC1,PC0]=01,4dB (Recommended)
[PC1,PC0]=10,12dB
[PC1,PC0]=11,0dB



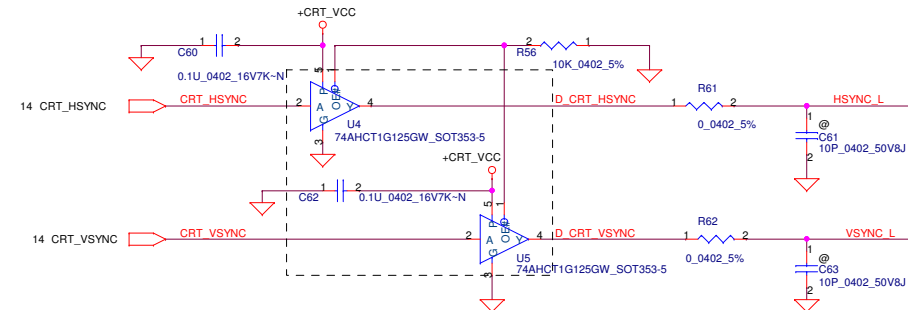
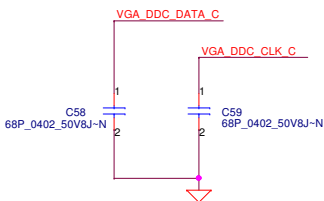
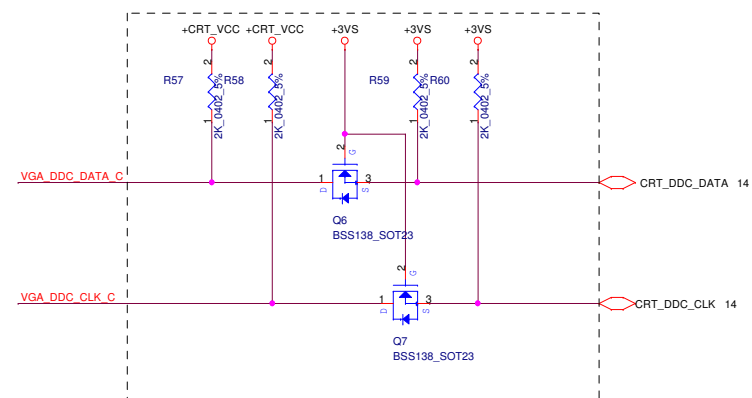
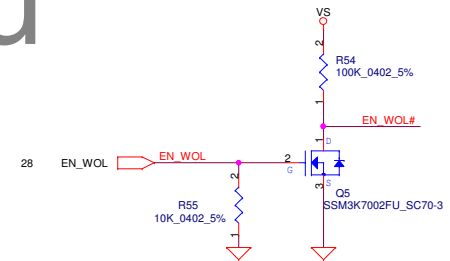
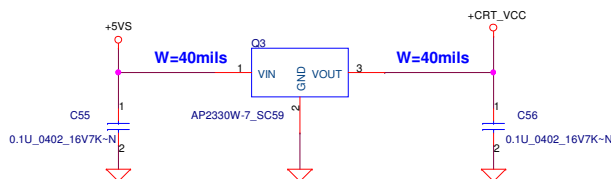
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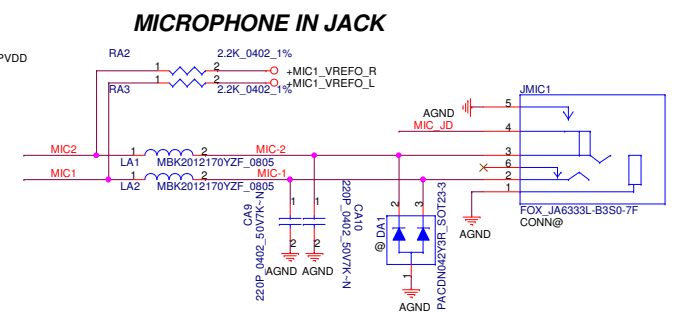
LAN / CRT CONN



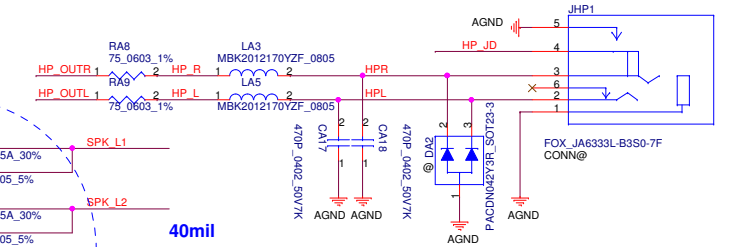
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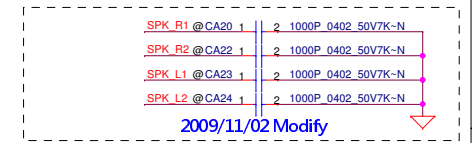
Security Classification	Compal Secret Data			Title	
Issued Date	2011/07/04	Deciphered Date	2012/07/04	LAN / CRT CONN	
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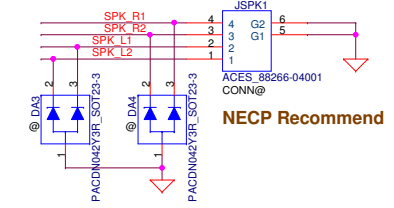
HEADPHONE OUT JACK



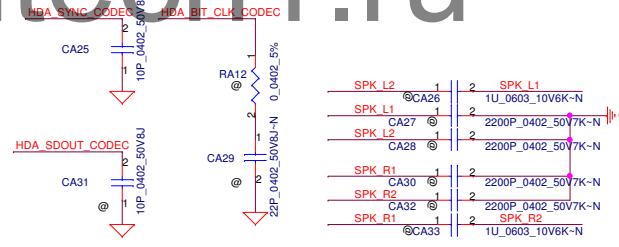
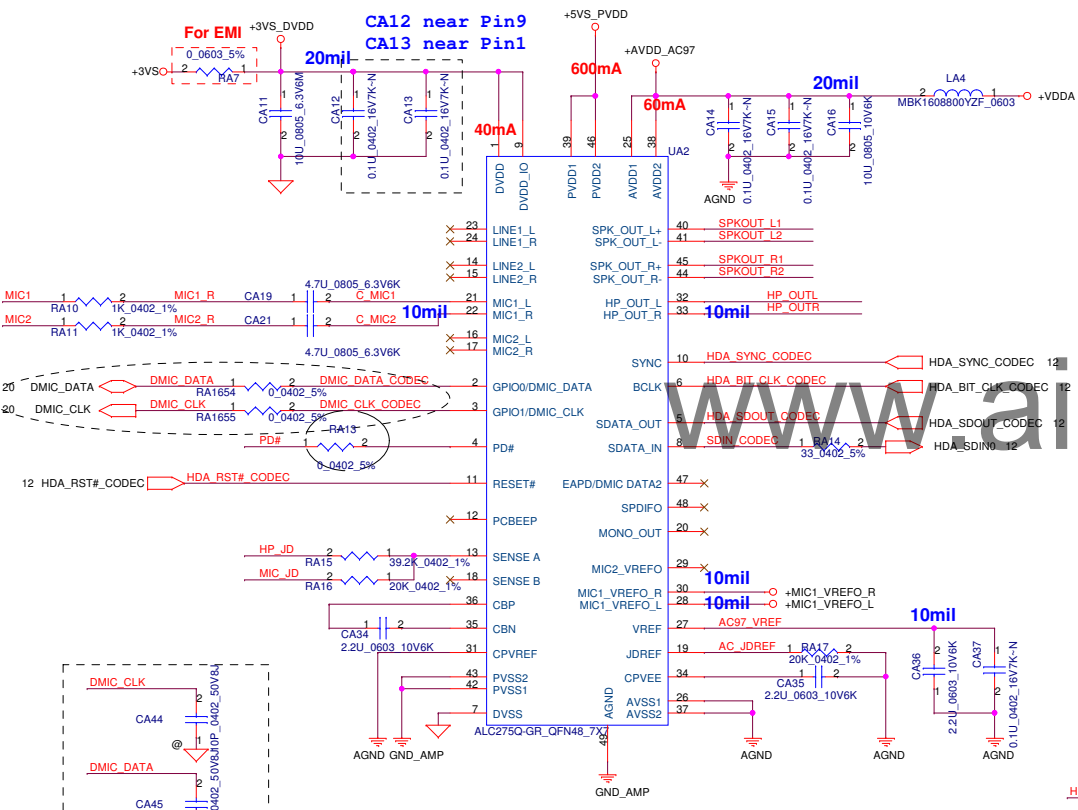
Speaker Connector



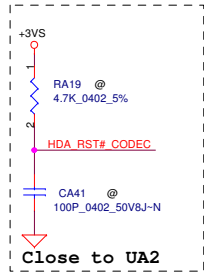
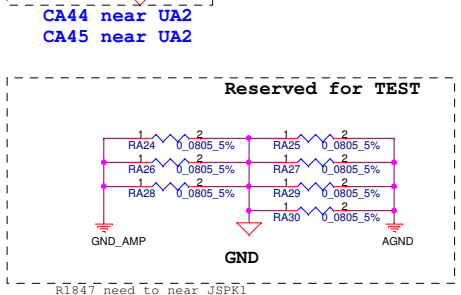
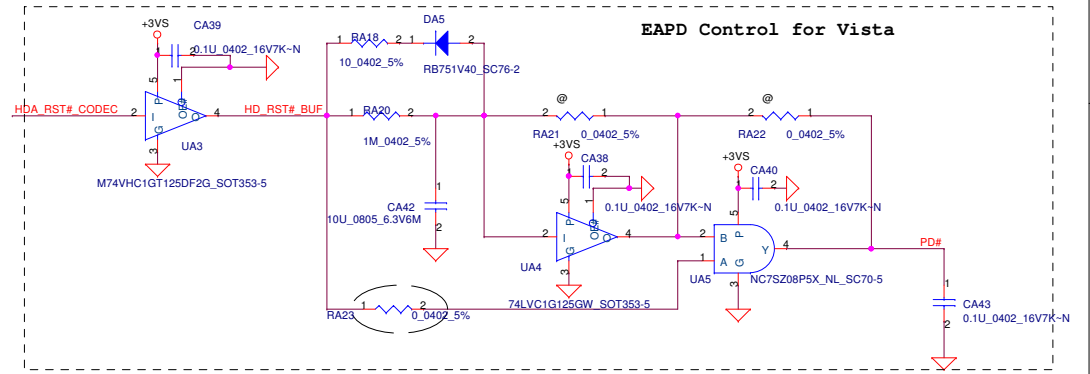
2009/11/02 Modify



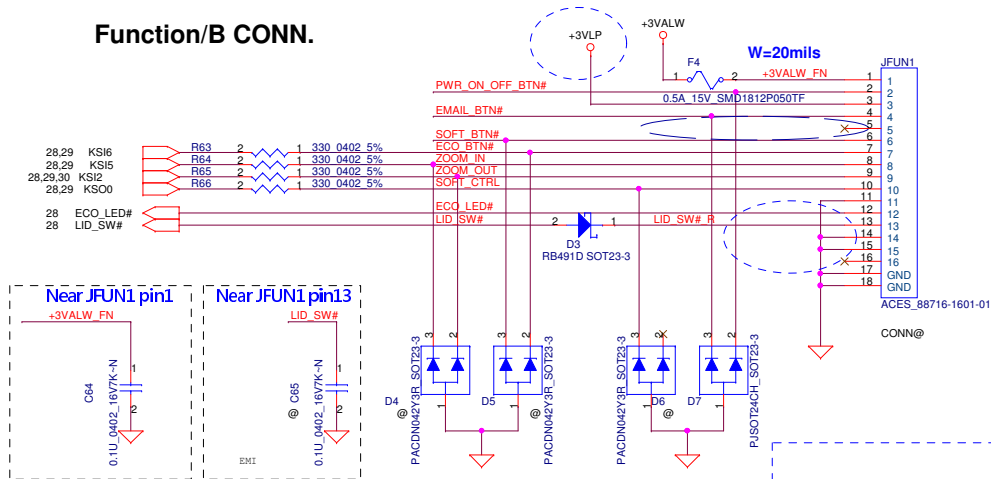
NECP Recommend



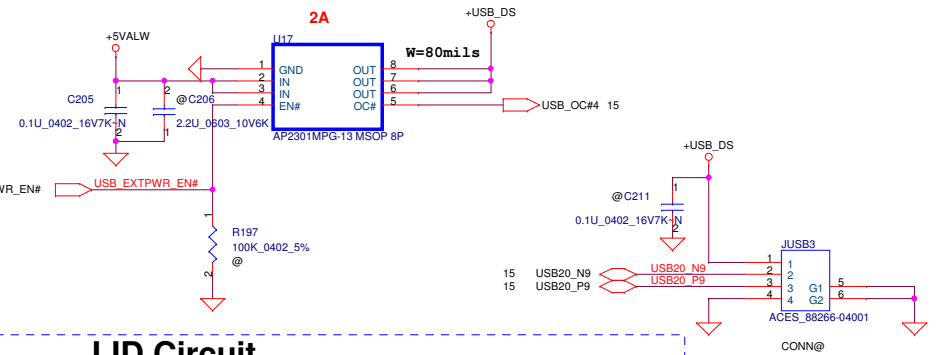
EAPD Control for Vista



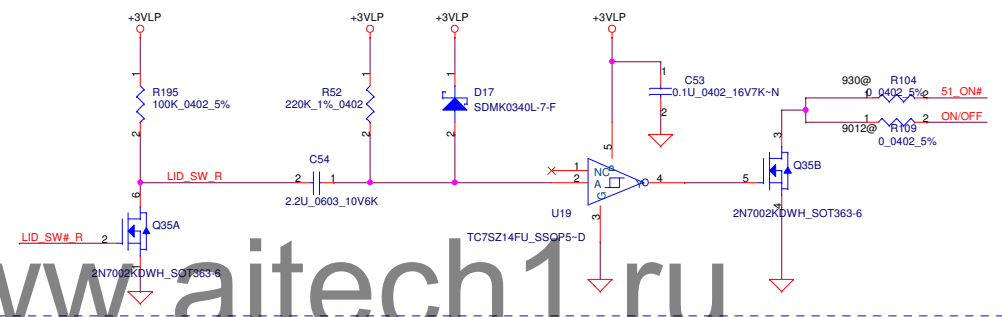
Function/B CONN.



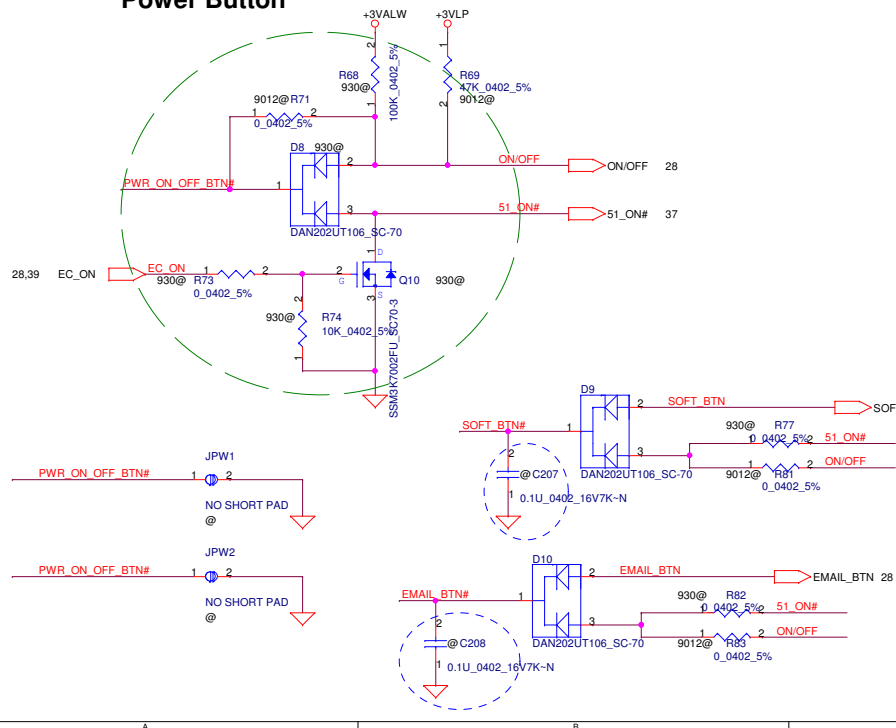
USB2.0/B CONN.



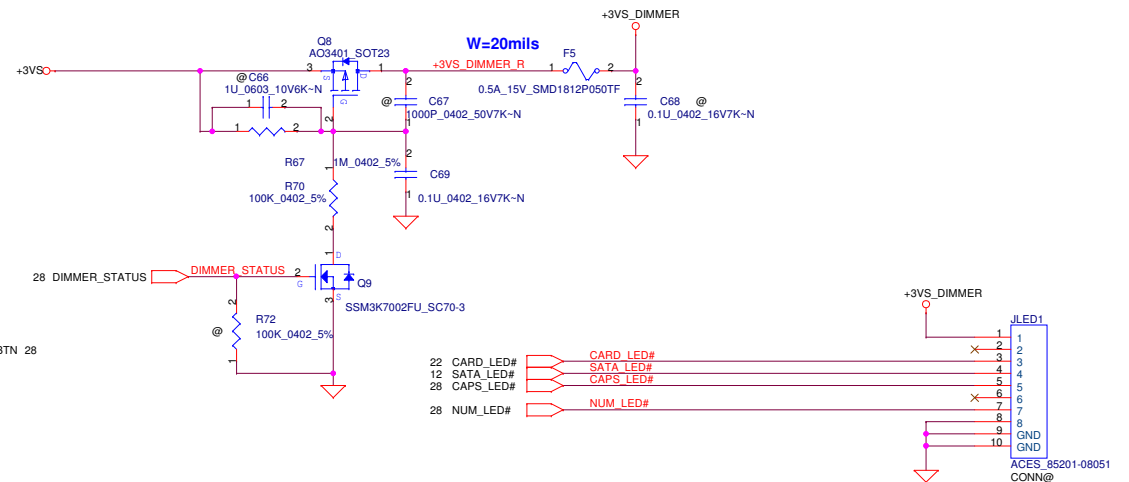
LID Circuit



Power Button



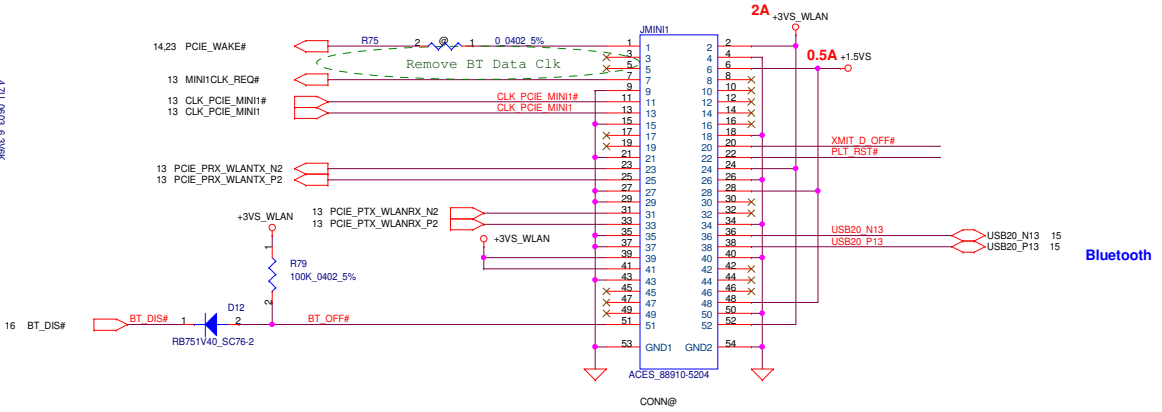
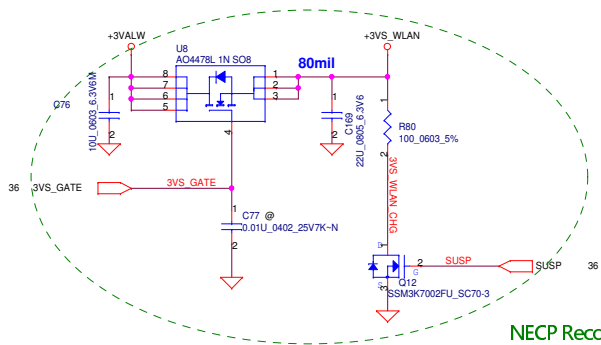
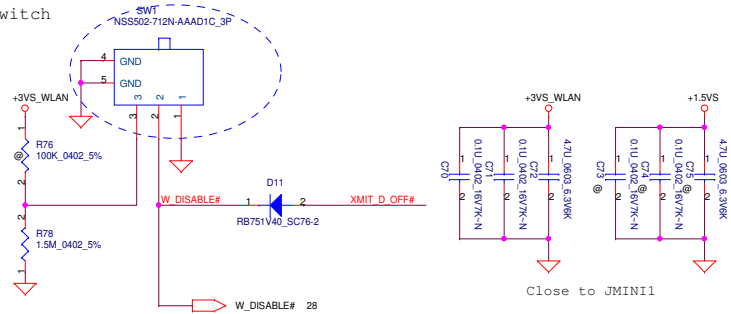
LED Circuit



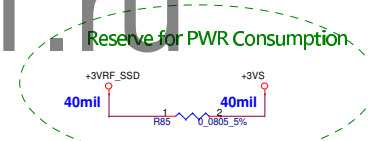
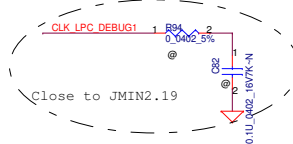
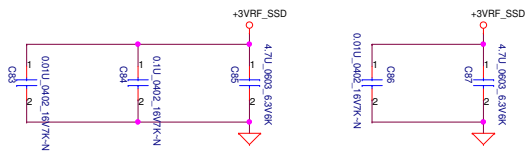
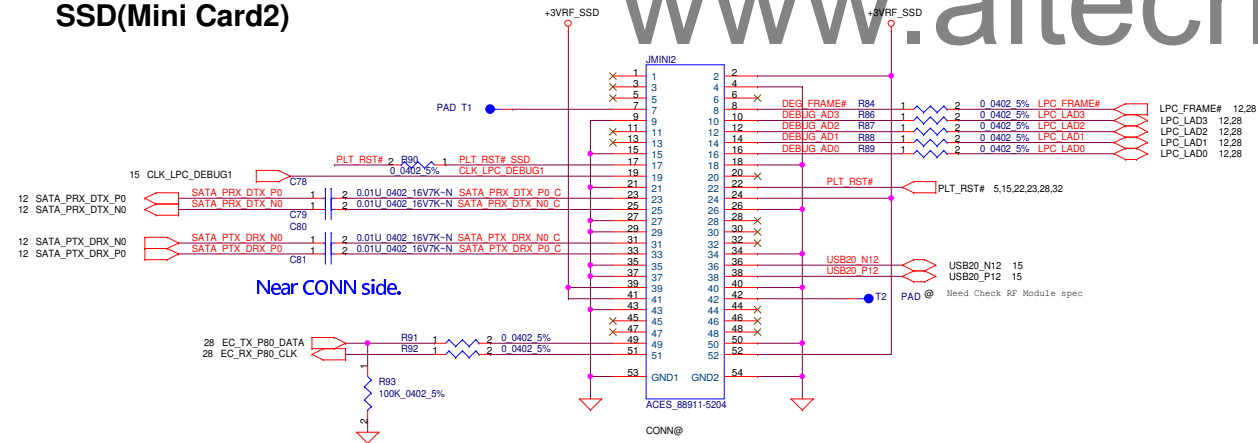
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WLAN (Mini Card1)

Killer switch

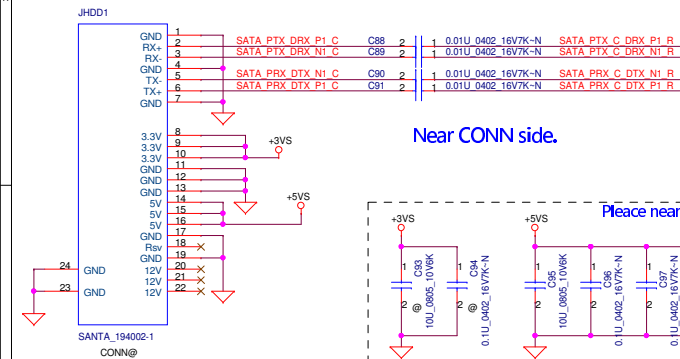


SSD(Mini Card2)

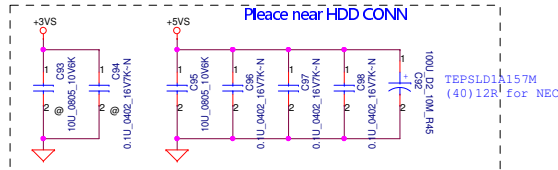


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		Deciphered Date		2012/07/04	
				WLAN/SSD	
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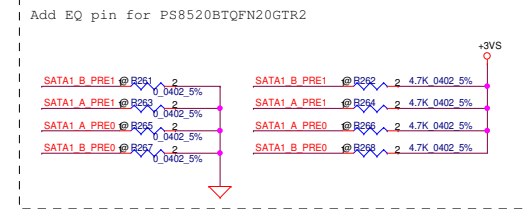
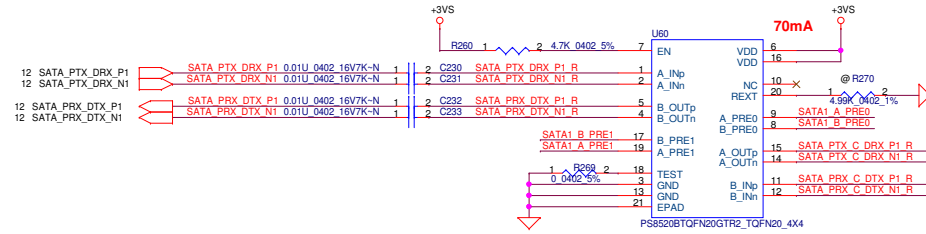
SATA HDD CONN.



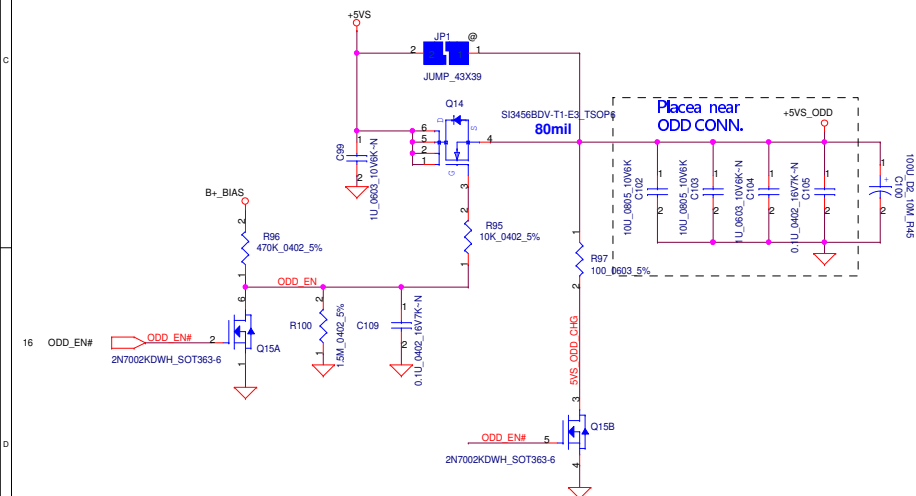
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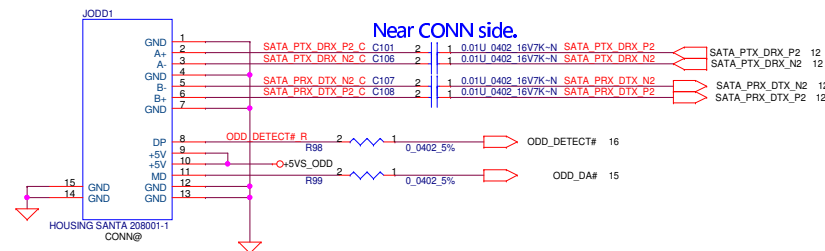
HDD-SATA Redriver



SATA ODD CONN.



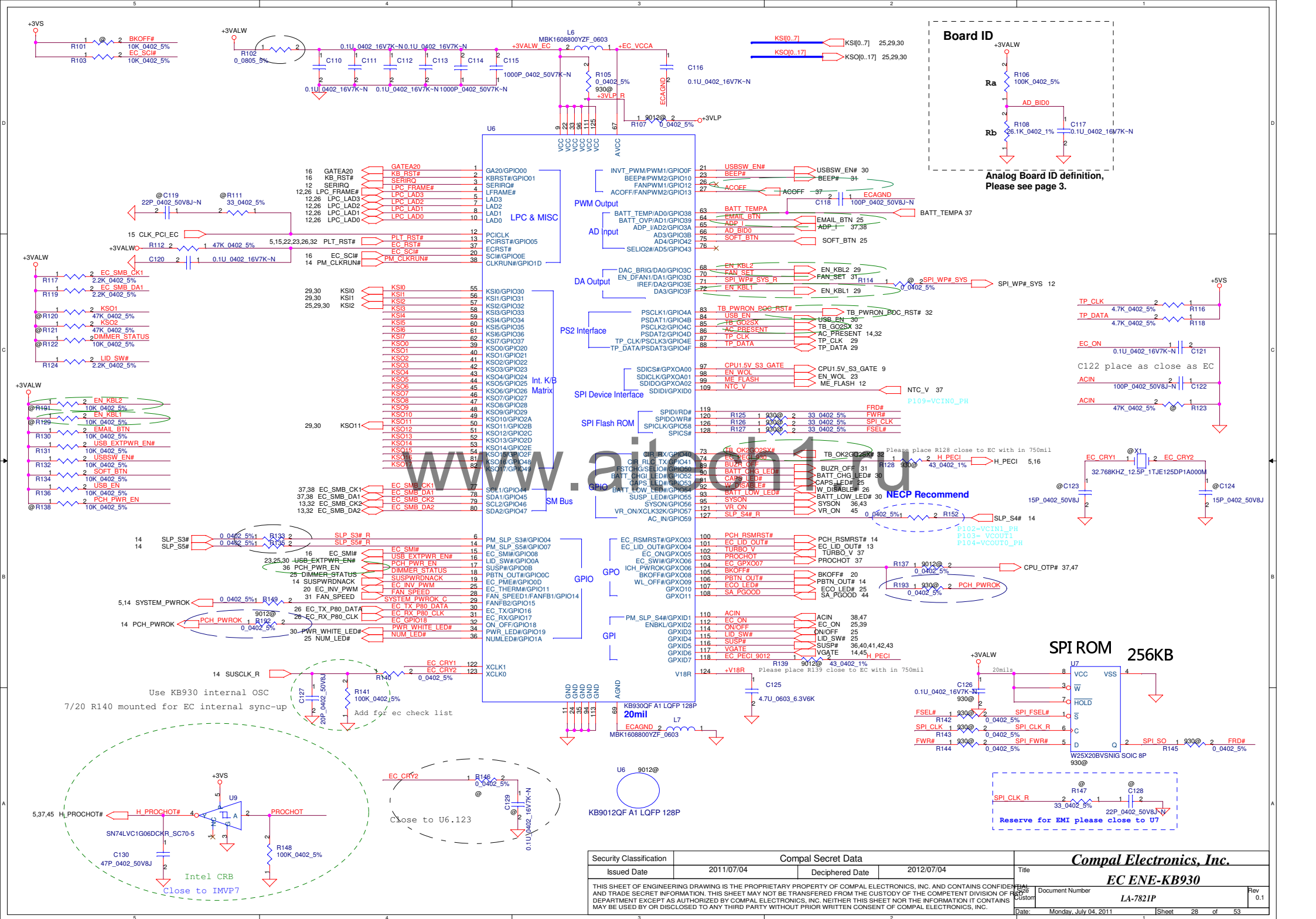
Place near ODD CONN.

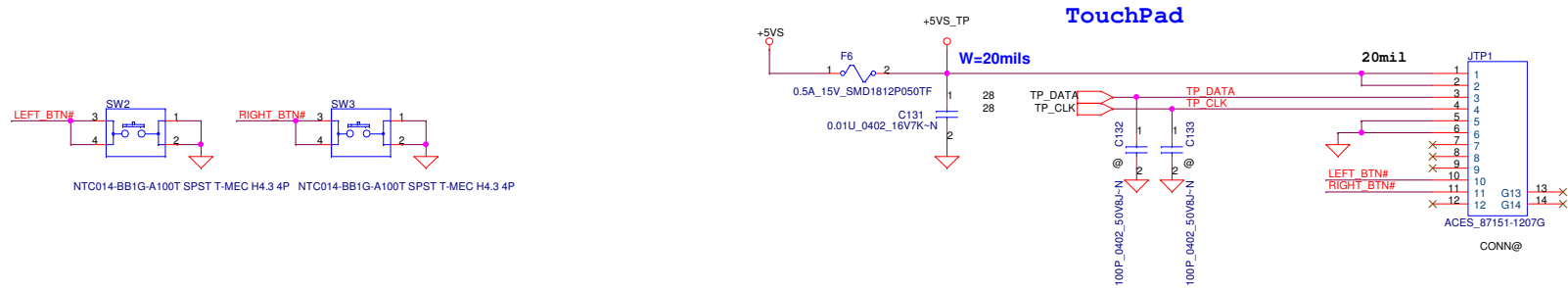


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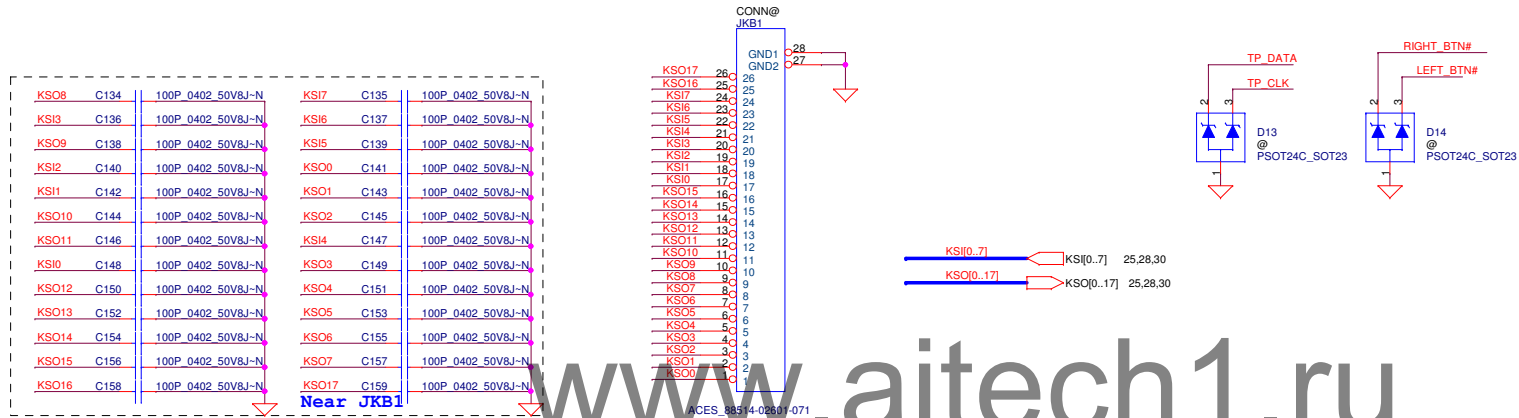
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Issued Date	2011/07/04	Deciphered Date	2012/07/04	Title	
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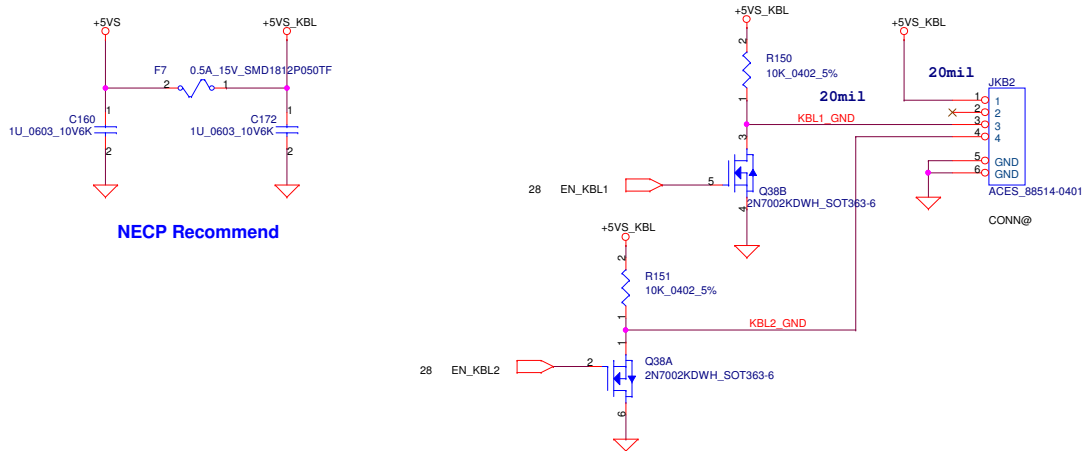




INT_KBD CONN.

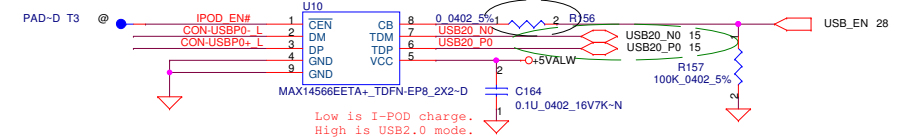
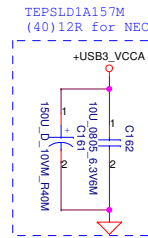
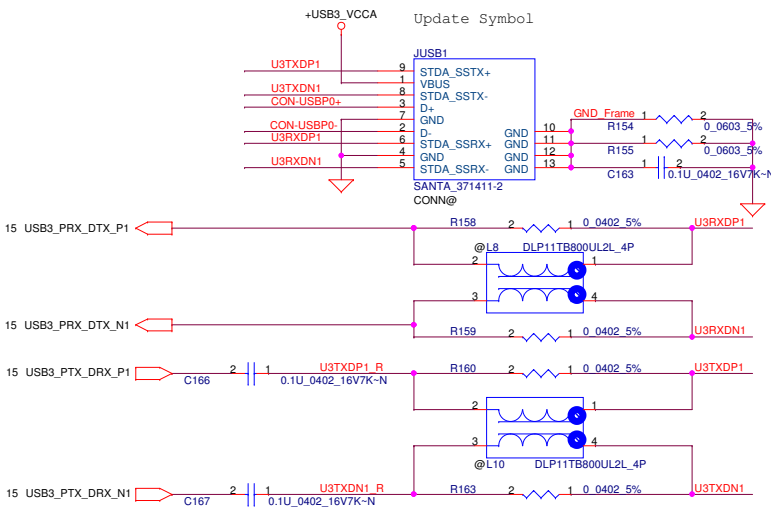
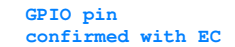


KB BackLight Control

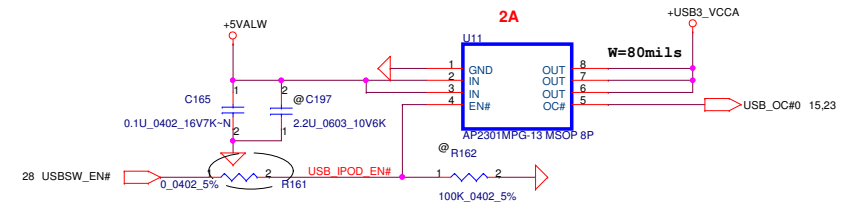
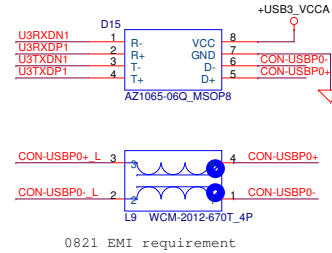


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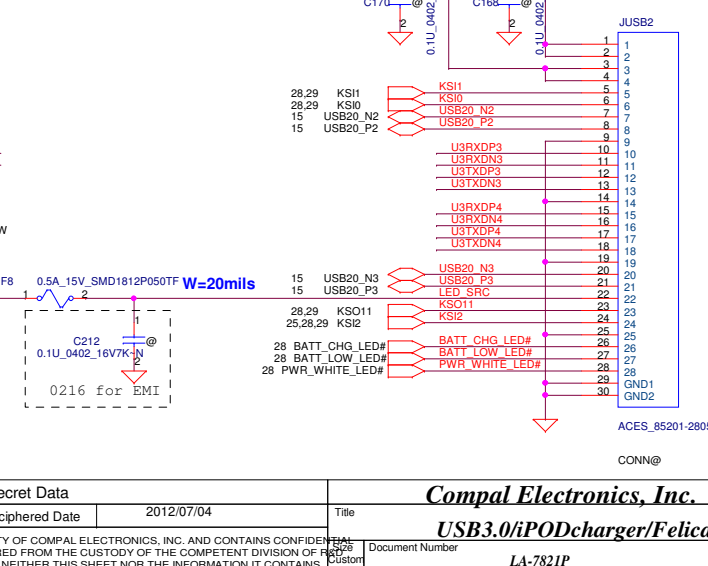
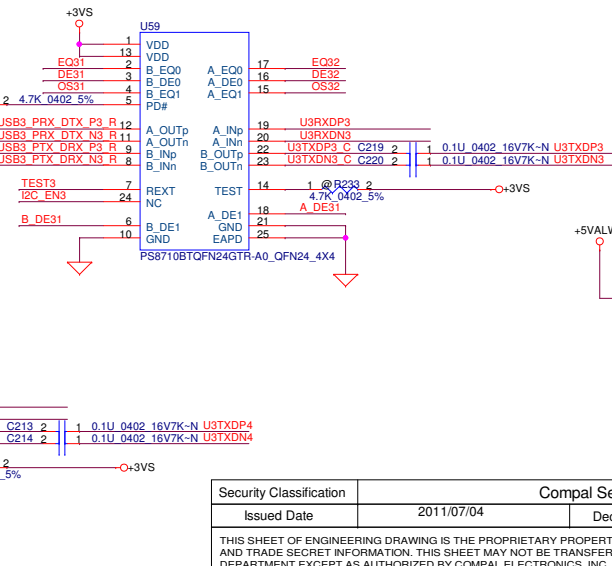
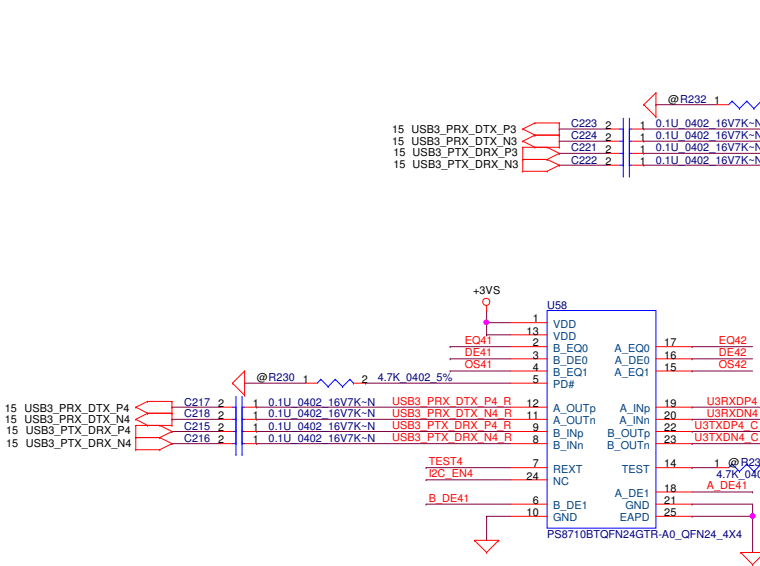
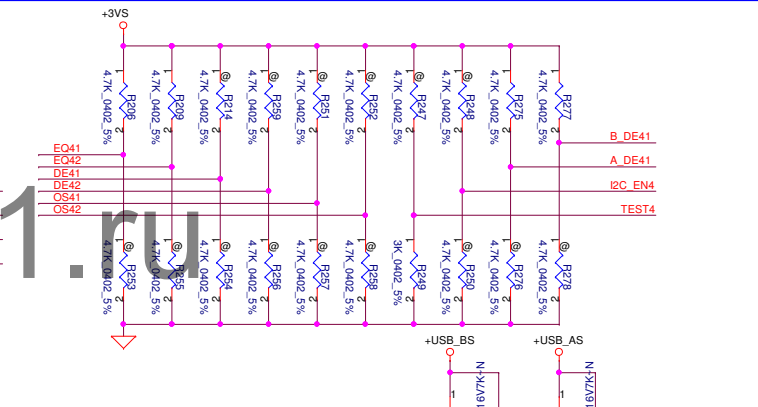
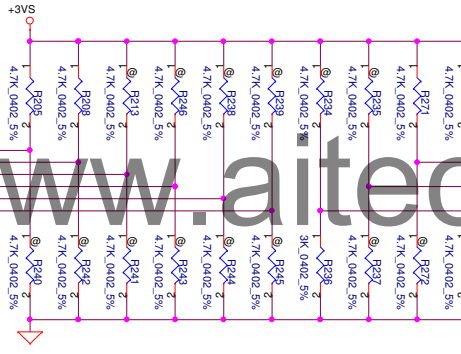
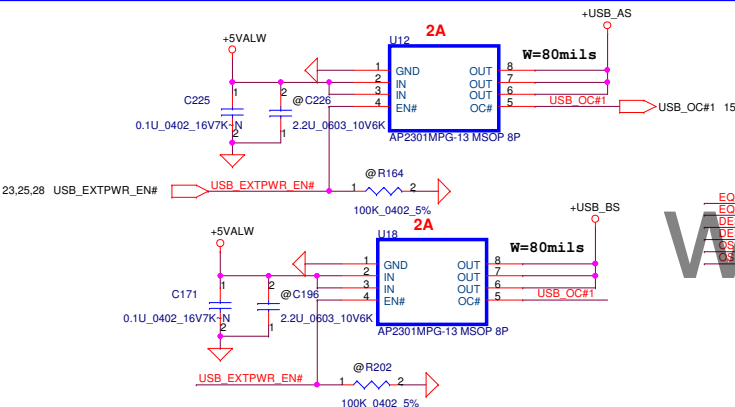
IPOD USB PWR SW



CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

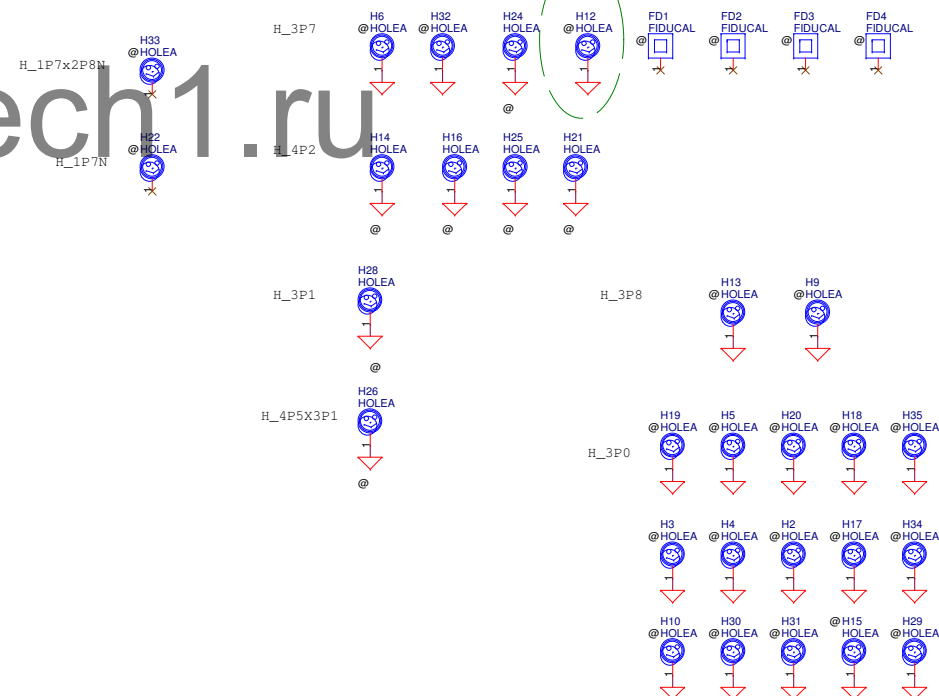


USB Sub Board CONN.

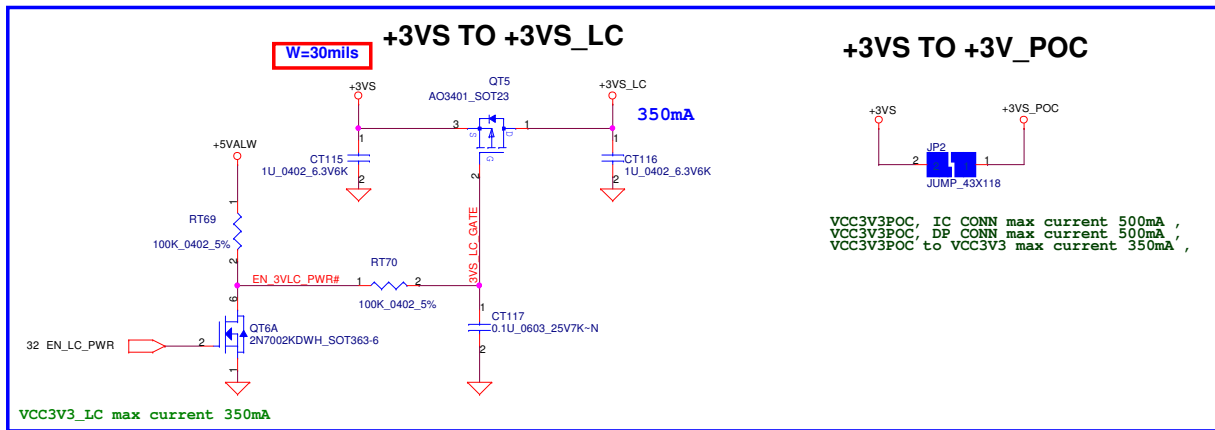


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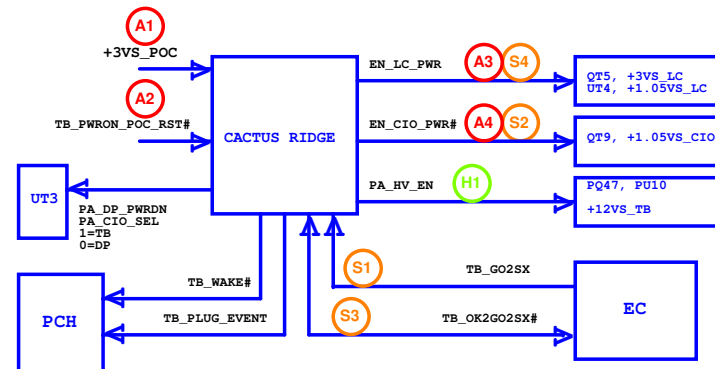
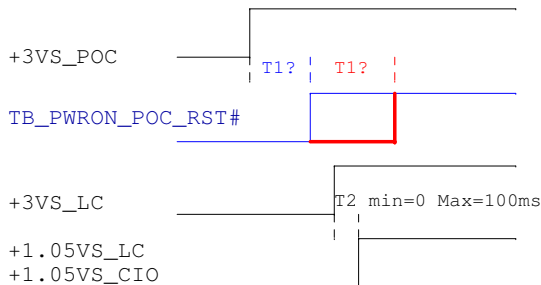
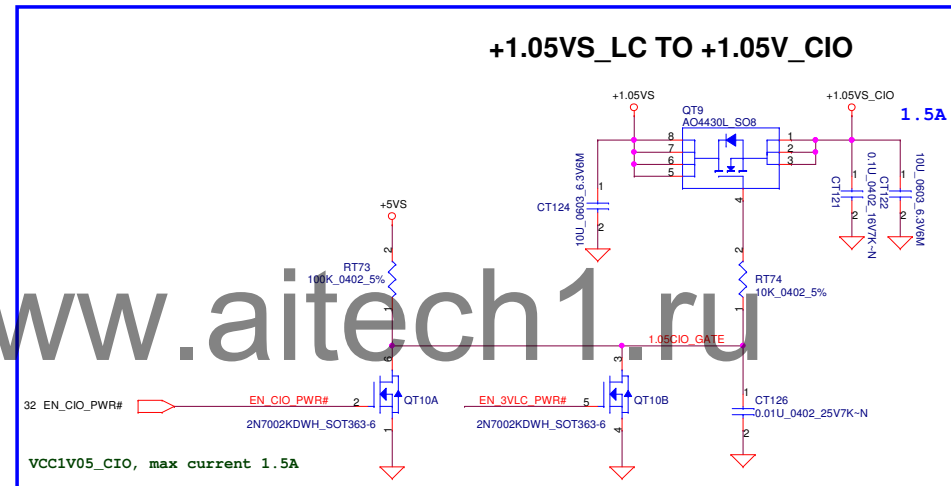
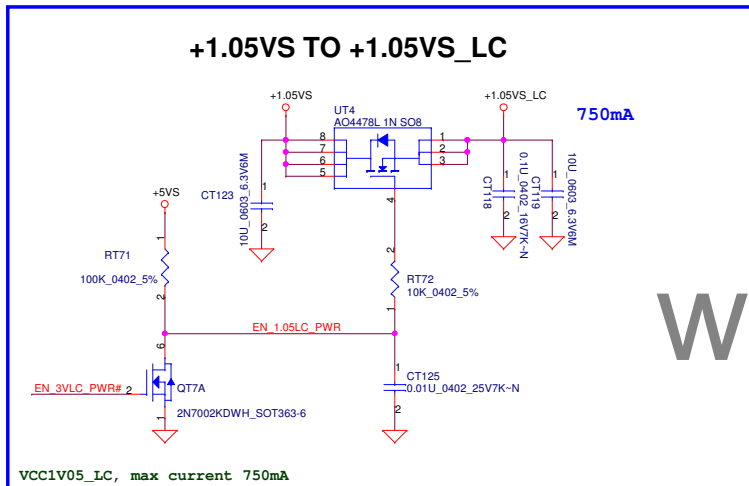
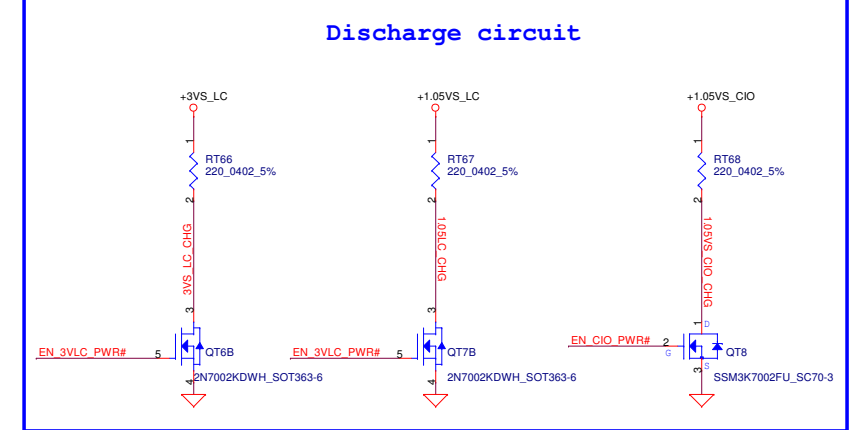
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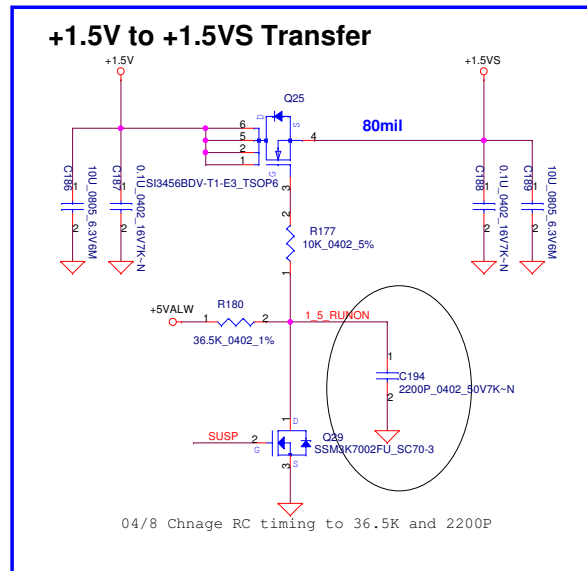
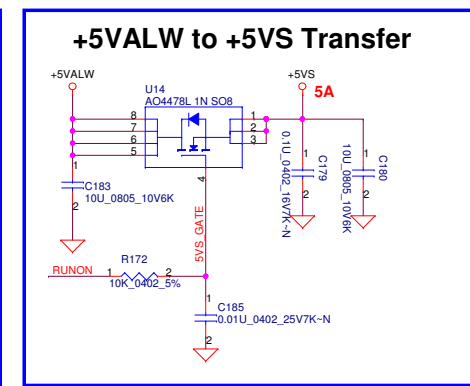
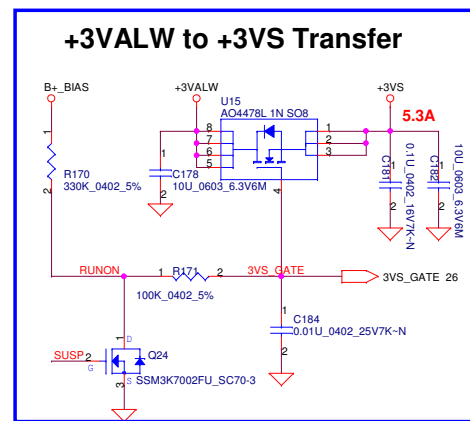
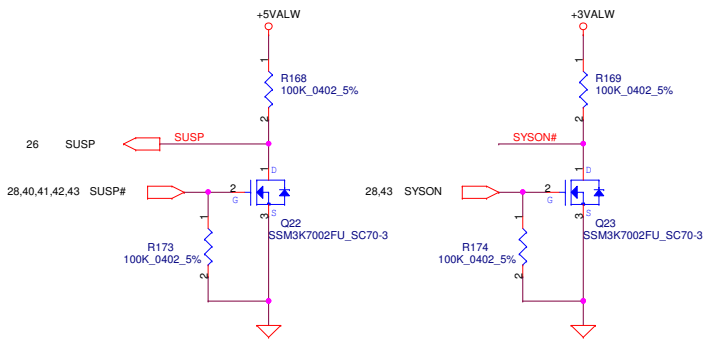
+3VS TO +3V_POC



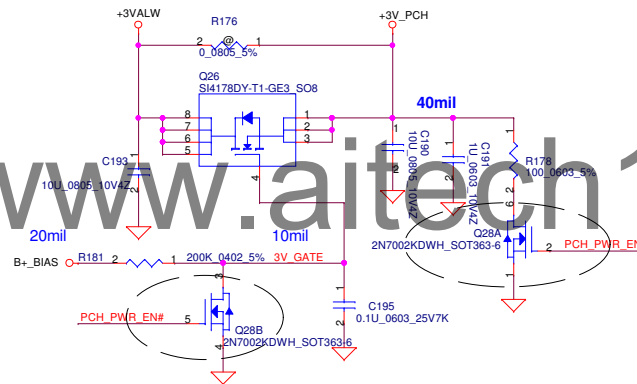
VCC3V3POC, IC CONN max current 500mA ,
VCC3V3POC, DP CONN max current 500mA ,
VCC3V3POC to VCC3V3 max current 350mA ,



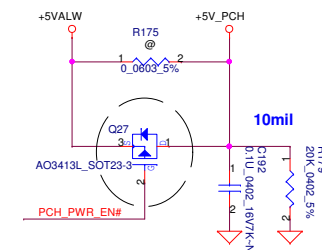
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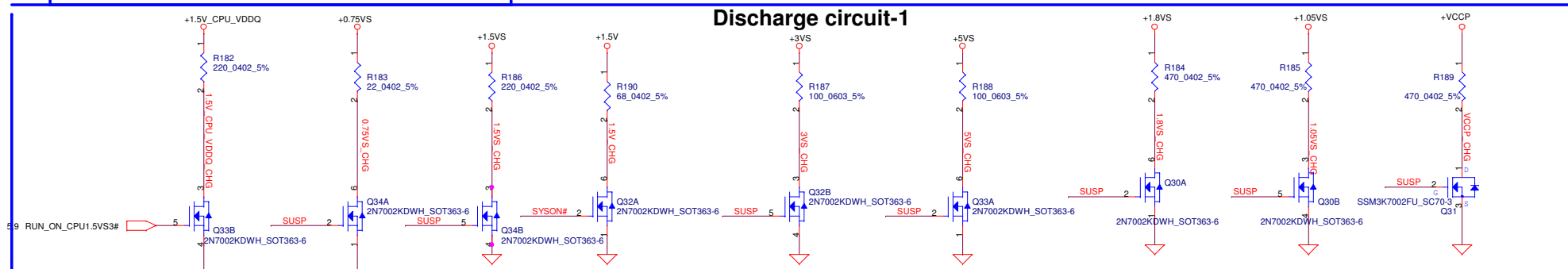
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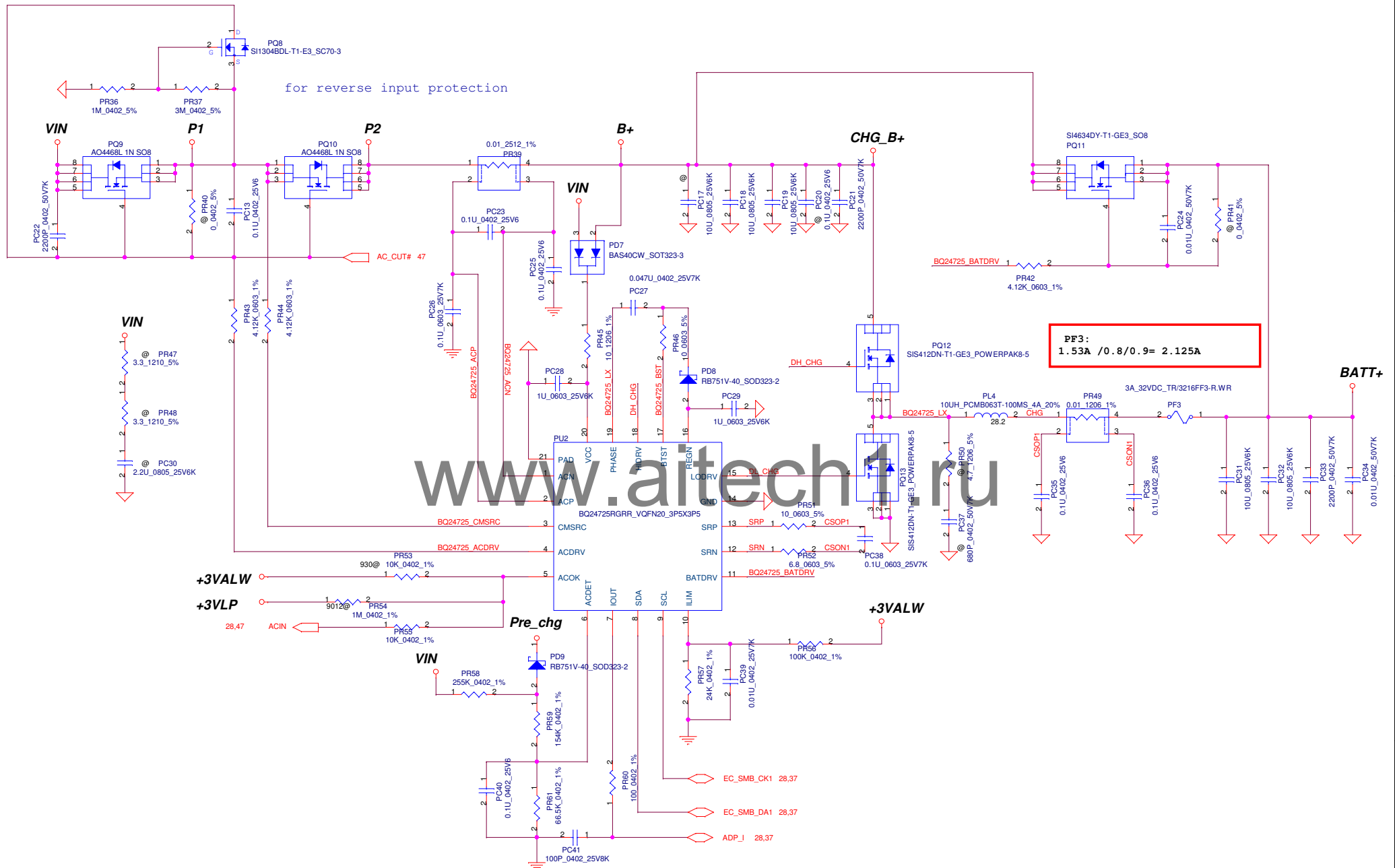
+5VALW TO +5VALW_PCH(PCH AUX Power)



Discharge circuit-1

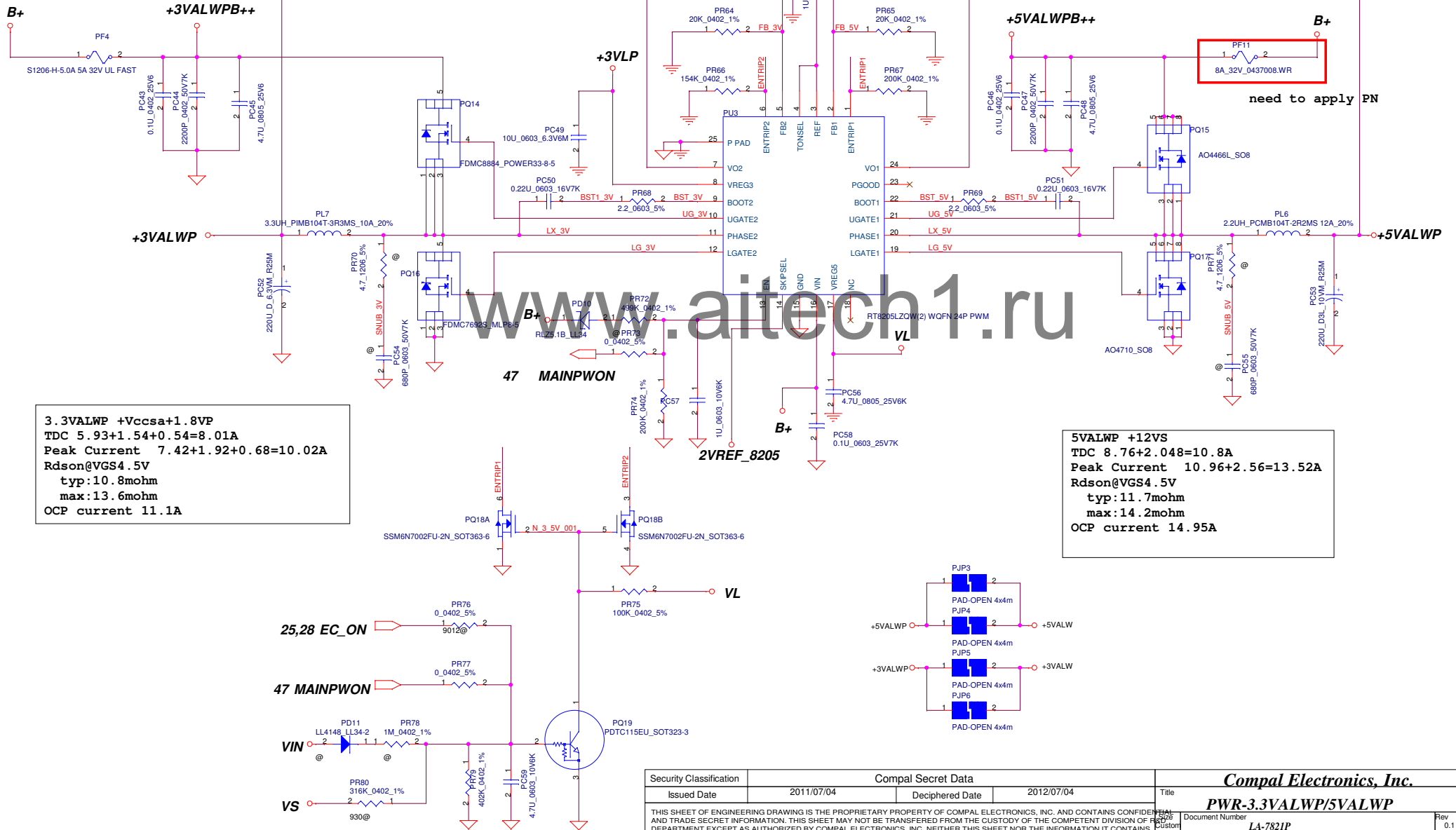


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PF4: $3.3V \cdot 8 = 26.4W / 0.85 = 31.06W$
 $2.58A / 0.8 / 0.9 = 3.59A$

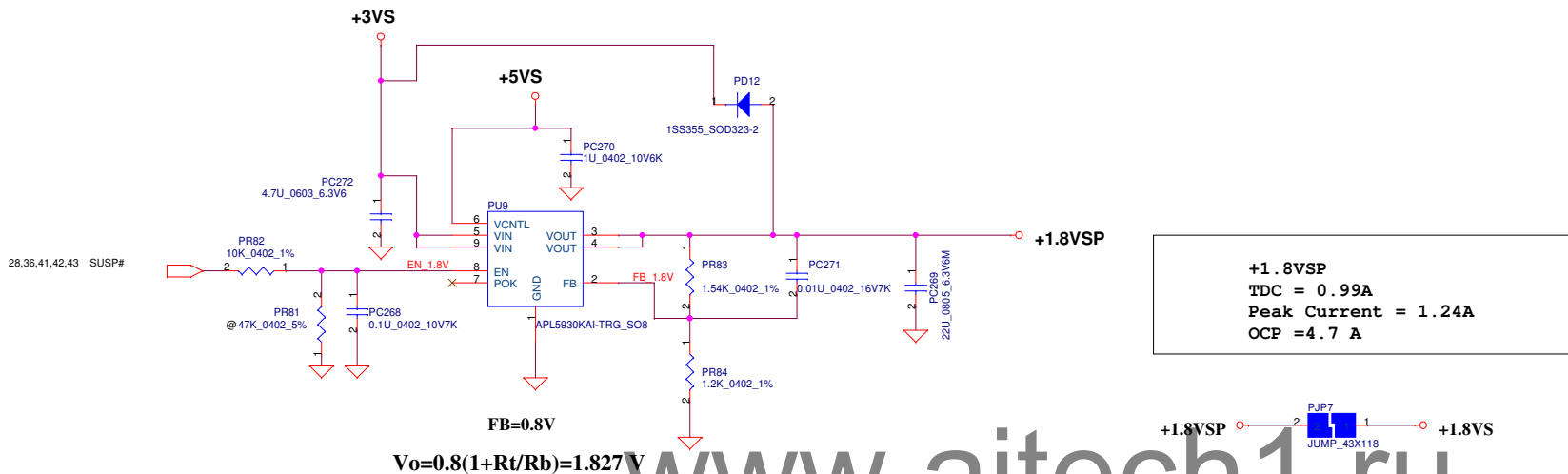
PF11: $5V \cdot 10.8 = 54W / 0.85 = 63.5W$
 $5.29A / 0.8 / 0.9 = 7.35A$



3.3VALWP +Vccsa+1.8VP
TDC $5.93 + 1.54 + 0.54 = 8.01A$
Peak Current $7.42 + 1.92 + 0.68 = 10.02A$
Rdson@VGS4.5V
typ: 10.8mohm
max: 13.6mohm
OCP current 11.1A

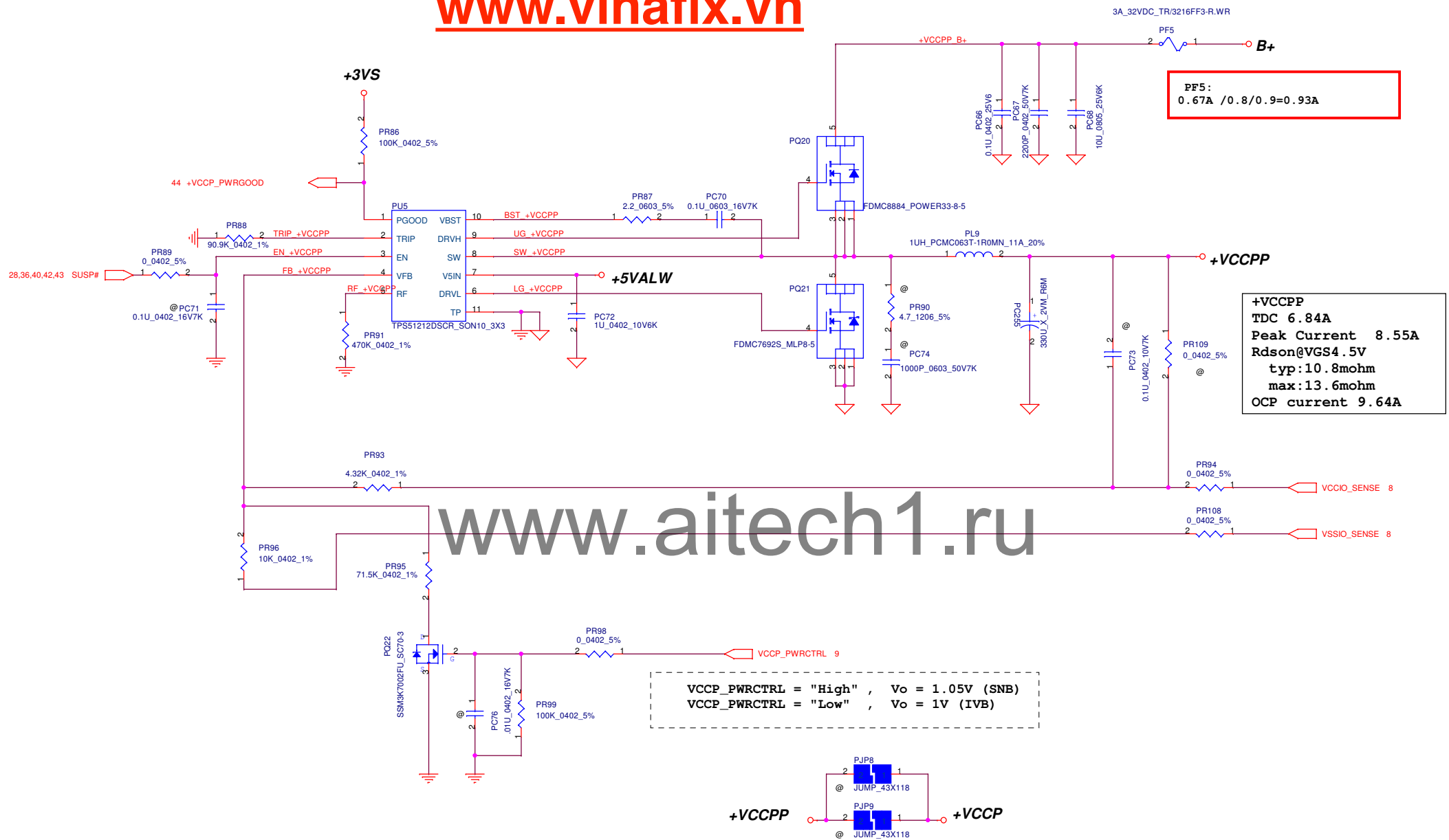
5VALWP +12VS
TDC $8.76 + 2.048 = 10.8A$
Peak Current $10.96 + 2.56 = 13.52A$
Rdson@VGS4.5V
typ: 11.7mohm
max: 14.2mohm
OCP current 14.95A

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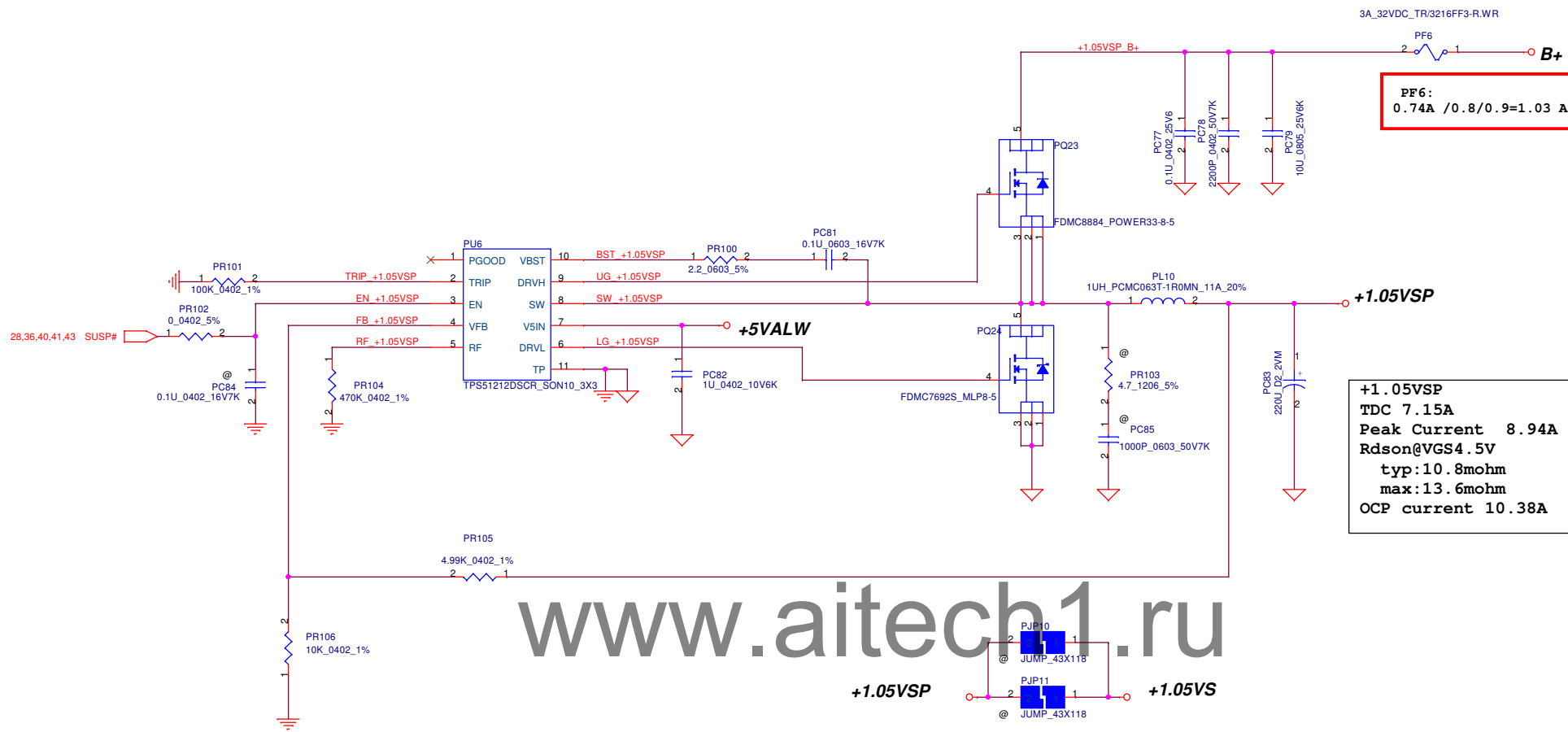


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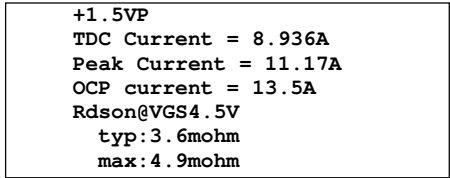


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PF7: $0.75v \cdot 1.2 + 1.5v \cdot 8.936 = 14.3W / 0.85 = 16.83$
 $1.4A / 0.8 / 0.9 = 1.95A$



+0.75VSP
TDC = 1.2A
Peak Current = 1.5A
OCP fixed to 1.6A

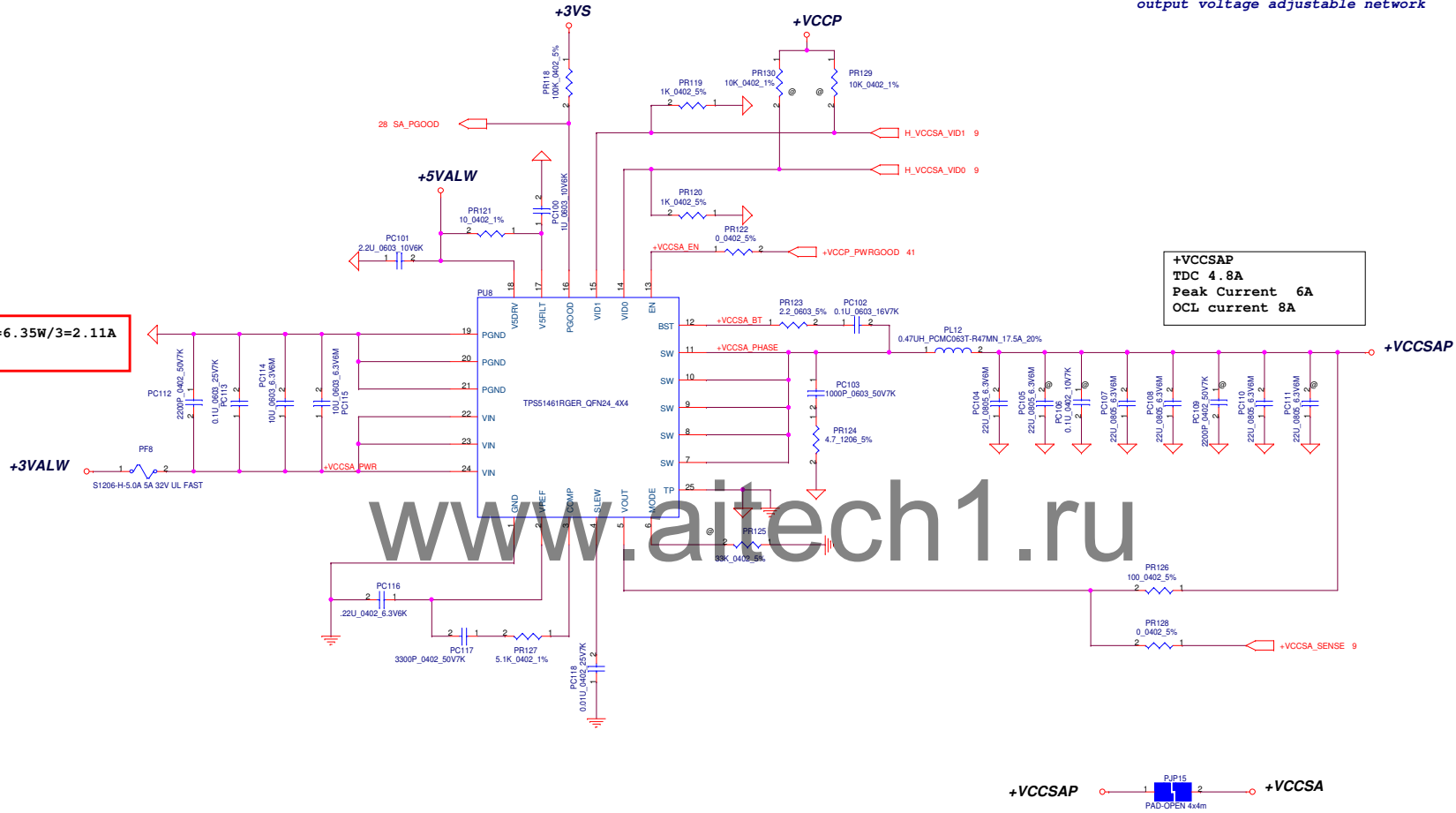
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$PF8: 0.9V \cdot 6A = 5.4 / 0.85 = 6.35W / 3 = 2.11A$
 $2.11A / 0.75 / 0.88 = 3.2A$

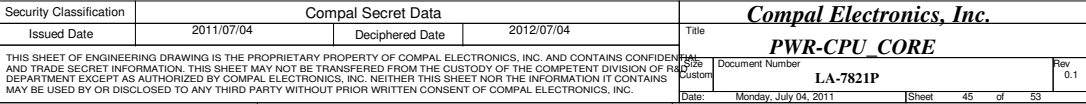
The 1k PD on the VCCSA VIDs are empty.
 These should be stuffed to ensure that
 VCCSA VID is 00 prior to VCCIO stability.

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

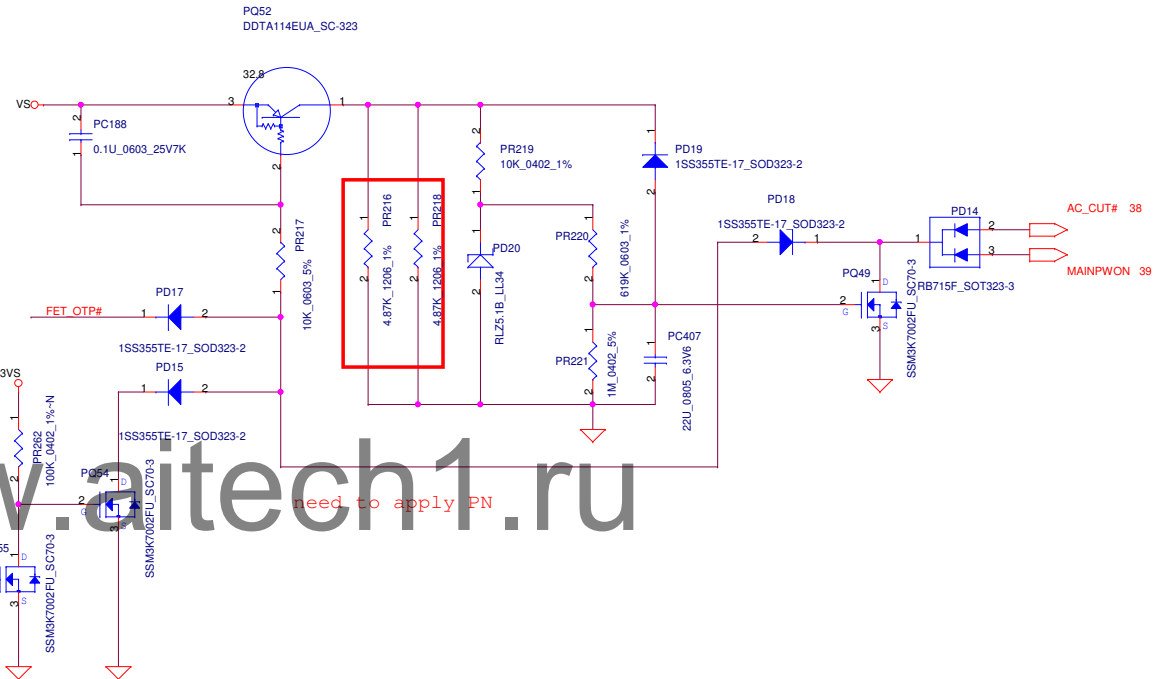
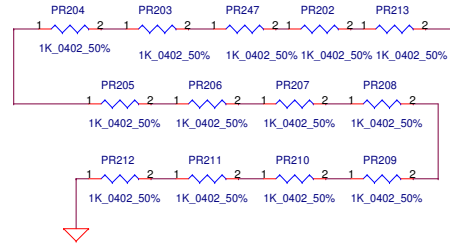
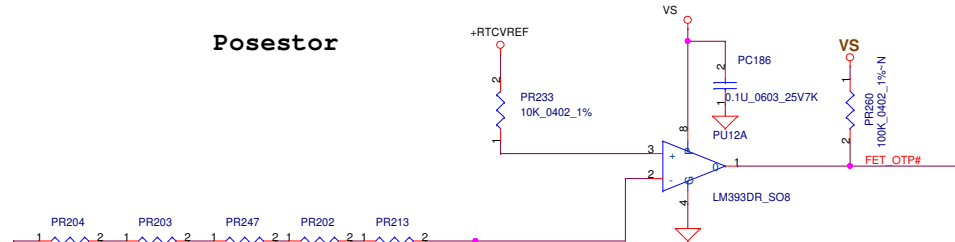
output voltage adjustable network



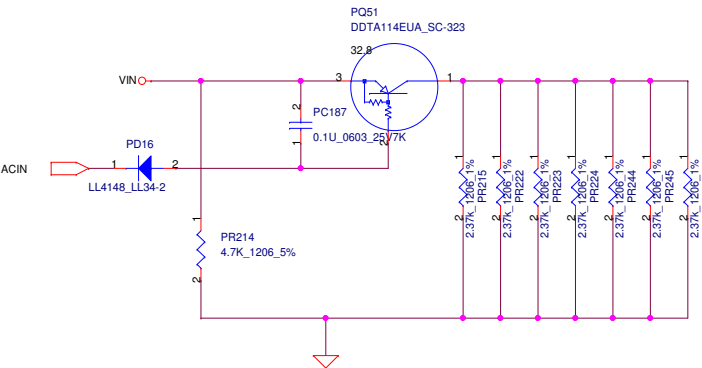
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Posestor



Remaining voltage discharge circuit request by NEC

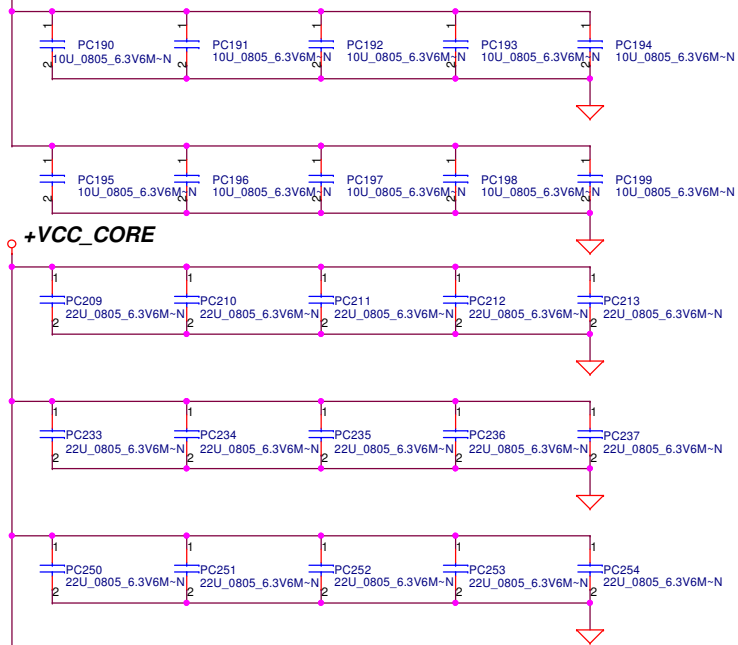


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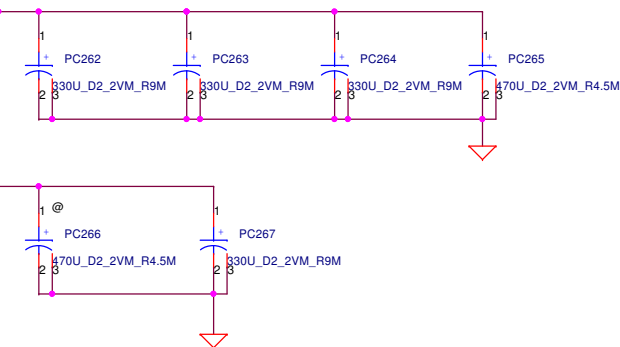
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+VCC_CORE

+VCC_CORE

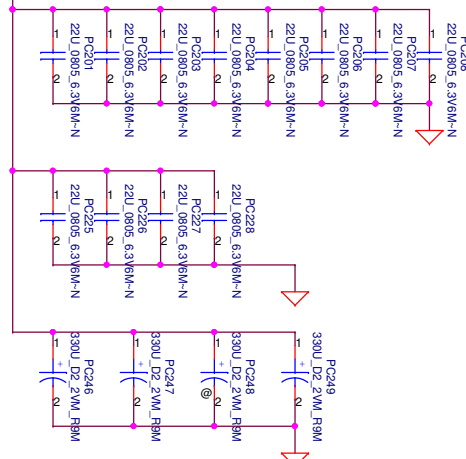


+VCC_CORE



+VCC_GFXCORE_AXG

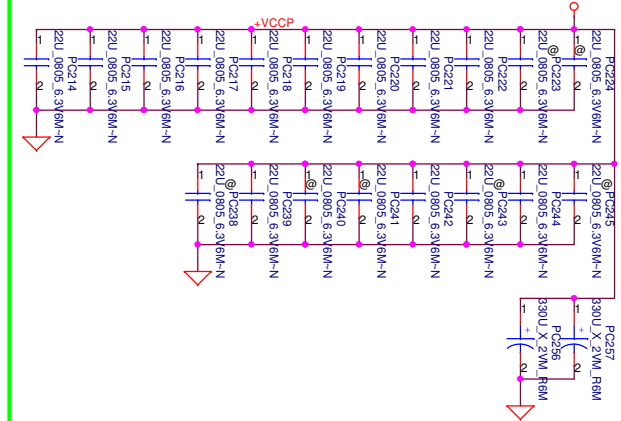
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+VCCP



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										Size Custom	
										Document Number	
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	41	VCCPP	11' 06/10	Compal_Aaron	change PC255 location	Location form page 46 to 41 :PC255	
2	43	1.5VP	11' 06/10	Compal_Aaron	Base on NECP request	Add PC405, PR270, PR271, PR97	
3	42	1.05VSP	11' 06/10	Compal_Aaron	change footprint	Change (A0N6414L SB00000NW00 and A0N6788 SB00000P300) to (FDMC8884 SB00000JM00 and FDMC7692S SB00000N800) Location :PQ23,PQ24	
4	47	Prosestor	11' 06/13	Compal_Aaron	add discharge commom circuit by NECP	Add PQ51,PD16,PC187,PR214,PR215,PR222,PR223,PR224,PR244,PR245,PR246	
5	47	Prosestor	11' 06/13	Compal_Aaron	add delay & latch commom circuit by NECP	Add PD14,PD15,PD17,PD18,PD19,PD20,PQ49,PQ52,PQ54,PQ55,PR262,PR263,PR217,PR216,PR218,PR219,PR220,PR221,PC188,PC407	
6	28	CHARGER	11' 06/13	Compal_Aaron	MOS derating	Change (SB00000HN00 MOS SI4172DY) to (SB00000DA00 MOS SI4634DY) Location :PQ11	
7	37	DCIN / BATT CONN	11' 06/15	Compal_Aaron	adjust OTP	Change (SB00000DH00 DMN66D0LDW-7_SOT363-6) to (SB000009610 SSM3K7002FU SC70-3) Location :PQ1	
8	43	1.5VP	11' 06/20	Compal_Aaron	remove PR92	remove PR92	
9	45	CPU_CORE	11' 06/20	Compal_Aaron	remove PC723	remove PC723	
10	39	3.3VALWP/5VALWP	11' 06/20	Compal_Aaron	adjust OCP	Change (SD034169380 S RES 1/16W 169K +-1% 0402) to (SD034178380 RES 1/16W 178K +-1% 0402) Location :PR67	
11	46	12VSP_TB	11' 06/20	Compal_Aaron	add OVP circuit by NECP	Add PQ50,PQ53,PR254,PR261,PR235,PR236,PR237	
12	44	VCCSAP	11' 06/23	Compal_Aaron	pull high resistor	Add PR129,PR130	
13	39	3.3VALWP/5VALWP	11' 06/24	Compal_Aaron	add PF11 by NECP	add PF11	
14	37	DCIN / BATT CONN	11' 06/27	Compal_Aaron	add PD22 by NECP	add PD22	
15	46	12VSP_TB	11' 06/28	Compal_Aaron	add PC294,PC295,PC296,PC297,PC298,PC299,PC300,PC301	add PC294,PC295,PC296,PC297,PC298,PC299,PC300,PC301	
16	45	CPU_CORE	11' 06/28	Compal_Aaron	remove PC724	remove PC724	
17	47	Prosestor	11' 06/29	Compal_Aaron	add posistor PR213,PR247 for PQ9 and PQ11 by NECP	add PR213,PR247	
18	40	1.8VSP	11' 07/04	Compal_Aaron	for current limit	Change (SD028000080 S RES 1/16W 0 +-1% 0402) to (SD034100280 RES 1/16W 10K +-1% 0402) Location :PR82	
19	39	3.3VALWP/5VALWP	11' 07/04	Compal_Aaron	adjust OCP	Change (SD034178380 RES 1/16W 178K +-1% 0402) to (SD034200380 RES 1/16W 200K +-1% 0402) Location :PR67	

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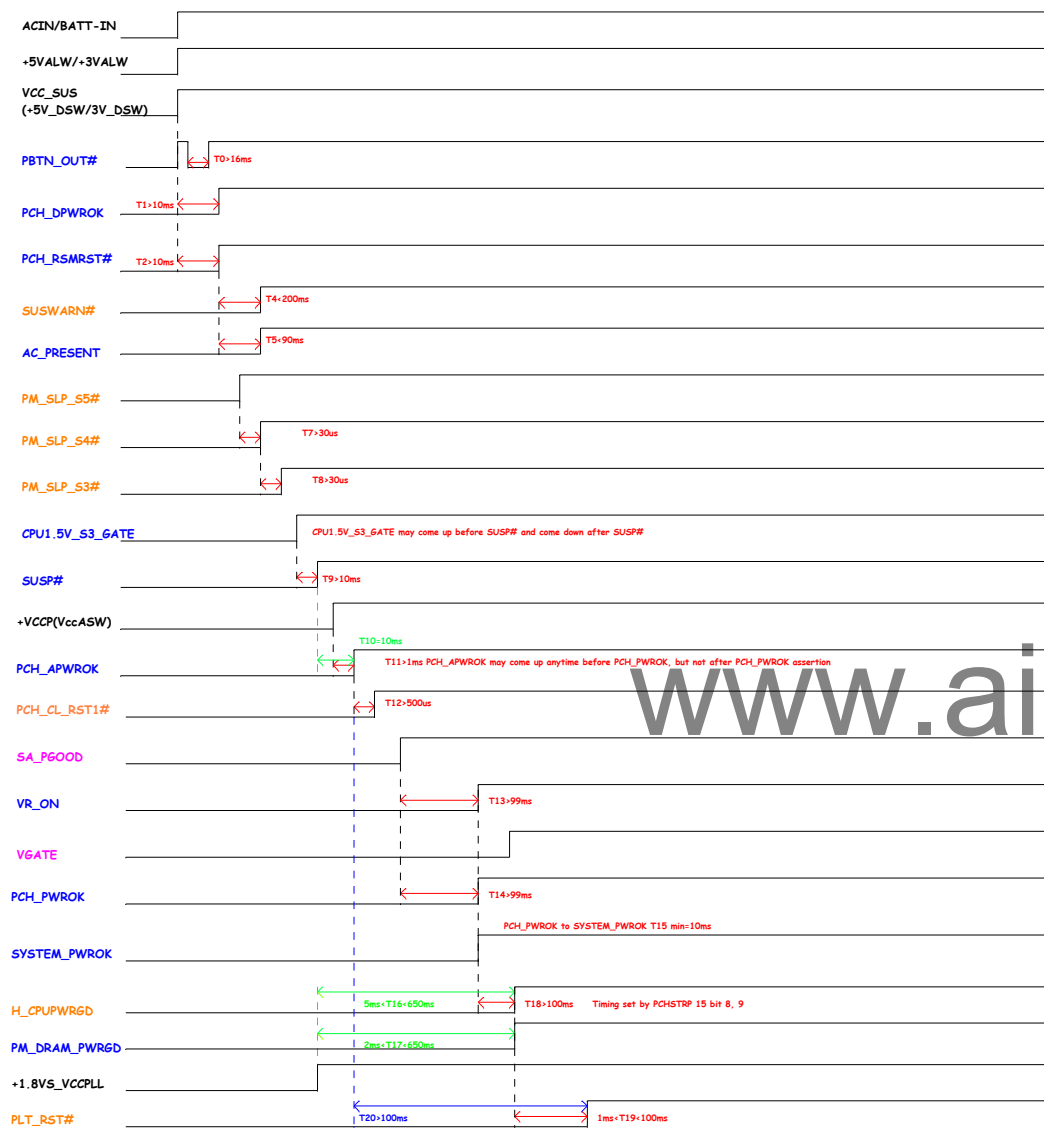
Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design	0.01	27	Swap SATA_PRX_DTX_N1 to SATA_PRX_DTX_P1	6/07	ES1
2		HW Design	0.01	04-09	Change JCPU1 Footprint to SUYIN_100361HK989J2R1PP	6/07	ES1
3		HW Design	0.01	33	Change RT56 to 1M from 10K ohm Change QT4 to BSS138 from 2N7002	6/07	ES1
4		HW Design	0.01	26	Add CI69 220 Change Q11 SI3456BD to U8 A04478L	6/08	ES1
5		ME Request	0.01	26	Change JUSB2 CONN ACES_87213 to PS_HPF10052	6/08	ES1
6		EMI Request	0.01	32	Add RT77 and CT120 close to UT2	6/08	ES1
7		NECP Recommend	0.01	12,20,28	Delete net CABC_EN, CABC_EN_C, CABC_EN_R	6/08	ES1
8		HW Design	0.01	23	Change Net name LANCLK_REQ# to +3VS	6/08	ES1
9		HW Design	0.01	28	Add RI92 for 90I20 Add R193 for 9300	6/08	ES1
10		NECP Recommend	0.02	29	Add +5VS_KBL2 circuit for KB Backlight Add Discharge circuit for +5VS_KBL1 and +5VS_KBL2	6/08	ES1
11		HW Design	0.02	15 23	Add USB3.0 Port2 and USB3.0 circuit for CRT/B USB	6/13	ES1
12		HW Design	0.02	30	Add USB2.0 Port 9 for JUSB3	6/13	ES1
13		NECP Recommend	0.02	36	Change Q27 AO3419 to AO3413L Add Q36 and Change Q27 AO3419L to AO3413L	6/13	ES1
14		HW Design	0.02	33	Change Q13 to AO3407AL from AO3401 Move RT15 to Q13 pin2 and change to 1M ohm Move RT56 to 100K ohm from 1M ohm Add 0 ESL diode DT4, DT5, DT6, DT7	6/14	ES1
15		NECP Recommend	0.02	33	Add DT4, DT5, DT6, DT7 for mDPconn	6/14	ES1
16		NECP Recommend	0.02	14	Add UH5 ,CH4	6/14	ES1
17		NECP Recommend	0.02	35	Change Gate signal EN_LC_PWR# to EN_3VLC_PWR#	6/14	ES1
18		NECP Recommend	0.02	29	Add RI98, RI99, Q37, Q38 for discharge circuit Add C210 , C207 and pop R153	6/14	ES1
19		NECP Recommend	0.02	28	Add R152 on SLP_S4# for measure power sequence	6/14	ES1
20		NECP Recommend	0.02	15 30	Change USB Port8 to Port10 Add USB3.0 Port 3 and Pot4	6/14	ES1
21		NECP Recommend	0.02	20	Add F10 for +3VS Camera	6/14	ES1
22		HW Design	0.02	30	Change JUSB2 Conn 16 pin to 28 pin Add U58 U59 for USB3.0 Redriver	6/14	ES1
23		HW Design	0.02	23	Change JCRT1 30pin to 40pin	6/14	ES1
24		NECP Recommend	0.02	05 08	Change RC19 10K to 1K Add RC97 pull down 10 ohm	6/17	ES1
25		NECP Recommend	0.02	33	Change FT1 FUSE 0.5A to 1A	6/17	ES1
26		NECP Recommend	0.02	28	Delete R101	6/17	ES1

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		HW Design (Ref Cactus Ridge 1.0 schematic)	0.03	32	U2 Change to pu +3VS_POC from +3VS_LC	6/20	ES1
2		HW Design (Ref Cactus Ridge 1.0 schematic)	0.03	32	UT1A PCIE_RST_X_N Change to pu +3VS_POC from +3VS_LC	6/20	ES1
3		HW Design (Ref Cactus Ridge 1.0 schematic)	0.03	32	UT1A PCIE_GPI0 Change to pu +3VS_POC from +3VS_LC	6/20	ES1
4		HW Design (Ref Cactus Ridge 1.0 schematic)	0.03	33	Change QT1A, QT1B to pu +3VS_POC from +3VS_LC	6/20	ES1
5		HW Design	0.05	26	U1A Debug port Add RT79-RT82 Pu to +3VS_LC	6/22	ES1
6		HW Design	0.05	24	Add QT11, UT5 For TB_PLUG_EVENT function	6/22	ES1
7		HW Design	0.05	09	Add pu RT88 to +3VS_POC of PA_LSRX_LSOE1_R	6/22	ES1
8		HW Design	0.05	23 30	Add pd RT89 to GND of PA_LSTX_LSEO1_R	6/22	ES1
9		HW Design	0.05	25	Change SW1 1BS003-1211L to NSS502-712N-AAAD1C	6/23	ES1
10		HW Design	0.05	27	RA31-RA34 Co-lay LA6-LA9	6/23	ES1
11		NECP Recommend	0.05	29	Add CC151 0.1U for +V_SM_VREF_CNT	6/24	ES1
12		HW Design	0.06	25	Update PS8710BTQFN24GTR Symbol	6/27	ES1
13		HW Design	0.06	23 30	ADD R280~R283;R271~R274;R275~R278	6/27	ES1
14		HW Design	0.08	24 20	Add LID Circuit	7/01	ES1
15		HW Design	0.1	21	Add D3 Diode	7/04	ES1
16					Add SATA Redriver		
17					Update KB Backlight Control Circuit		
18					Add Q35 ,C207 ,C208		
19					ADD R280~R283;R271~R274;R275~R278		
20					ADD Add CA44, CA45, UA2 for EMI		
21					ADD Add C209, C210, UCM1 for EMI		
22					Add R40,R41 Only for ES1 verification		
23							

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Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by Intel® MVP
Signal Names	Voltage rails or chip-to-chip buses